MULTIPLIERLESS IMPLEMENTATION OF BANDPASS AND BANDSTOP RECURSIVE DIGITAL FILTERS USING LOW-SENSITIVITY TRANSFORMATION

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ABSTRACT

Multiplierless filters are natural extensions of the low-sensitivity structures. Some low-sensitivity transformations are investigated for converting a prototype lowpass filter into a bandpass or a bandstop filter. The resulting coefficient values, due to such transformations, become quite low compared with conventional structures. When the coefficient values are expressed in minimum signed powers of two (MNSPT) forms or canonic signed digit (CSD) forms, they require few shifts and adds and/or subtracts for implementation and a multiplierless realization can be obtained. Further, when we allow some marginally insignificant deviation in the specifications including the tolerances and the bandedges, the number of shifts and adds and/or subtracts per multiplier becomes quite small making this approach quite attractive. Alternatively, we can design the overall filter with marginally stricter tolerances than the desired specifications and meet the criteria after quantizing the coefficients.

1 INTRODUCTION

Minimum number of signed powers of two (MNSPT) or canonic signed digits (CSD) representations of binary digits are extensively used for representing the multiplier coefficients in multiplierless implementation of a digital filter. An MNSPT representation of a coefficient value is given by $\sum_i a_i 2^{-t_i}$, where each a_i is either 1 or –1 and t_i is a positive or negative integer. For instance, 1.93359375 can be realized as $2–2^{-4}–2^{-8}$. In this case, the multiplication is more efficiently and economically achieved with aid of three bit shifts and two subtracts, and not by a nine-bit multiplier.

The structures such as a sum of allpass filters, including attractive lattice wave digital (LWD) filters, coupled with optimization methods have shown to yield good results for multiplierless implementation [10–13, 17, 18] in the case of IIR filters. These sums of allpass filters are characterized by the attractive property that there exist structures with the number of required multipliers being equal to the filter order, thereby decreasing the number of multipliers compared to conventional realization forms.

A major approach for multiplierless implementation comprises of that of optimization [7–9, 17, 18], i.e., searching for the coefficients such that they can be implemented in MNSPT forms and the given criteria are still met. Optimization methods are used to find the optimal transfer functions under given constraints, filter design being basically a problem of approximation due to the tolerances in specifications. In general, the methods of optimizations are considered to be quite satisfactory. However, one may not assure or guarantee that the optimal solution will always be found under the given constraints. The solution can be unsatisfactory, for example, in terms of the filter order, the given wordlength of the multipliers, or the specified number of shifts and adds (in the case of multiplierless implementation), or some combination of them. Under such conditions, some parameters or characteristics of the filter will have to be relaxed to obtain an acceptable design and realization specific to the system it is intended to be used.

Another interesting approach is the one that stems from design of an odd-order elliptic minimal Q-factor analog filter (EMQF) that has some special properties. Using the bilinear transformation these filters can be implemented as a sum of two allpass filters [10-13]. This method may also be associated with an expanded design parameters space like passband (stopband) tolerances, edges, and the filter order.

Especially, in the case of FIR filters, another approach is based on combining simple sub-filters that can be implemented using only few shifts and adds and/or subtracts. Although quite attractive, to make this approach as a viable one, a large database of such filters will have to be generated and some optimization method will have to be evolved in order to combine some of them to meet the desired specifications.

The feasibility of implementing multiplierless recursive digital filters based on coefficient translation methods in low-sensitivity structures has been demonstrated in [2, 3]. These low-sensitivity structures are based on replacing the unit delay element by a simple structure that is equivalent

of shifting the origin of the *z*–plane [1, 4]. When implemented in MNSPT forms or CSD forms, the modified coefficients require few shifts and adds and/or subtracts for implementation. Allowing a marginally insignificant deviation in specifications a gross reduction in number of nonzero bits (effectively the number of shifts and adds and/or subtracts required) has been seen to be feasible.

We observe that the low-sensitivity transformation substitution blocks in [5] is somewhat akin to that of coefficient translation methods in a sense that the shift of the origin is not in the *z*–plane but in the *v*–plane [1, 4, 5]. These transformations become potential candidates for investigating for generating multiplierless implementations, which is the main topic of this paper.

2 THE STRUCTURES FOR IMPLEMENTATION

One of the design and implementation methods for bandpass filters (BPF) or bandstop filters (BSF) comprises that of designing a prototype lowpass filter (LPF) first followed by an appropriate frequency transformation [6]. In order to gain the advantage of the reduced number of multipliers, and also to avoid delay-free loops due the transformed block, one would prefer using the following substitution [6]:

$$z^{-1} \to -(z^{-2} - \alpha z^{-1})/(1 - \alpha z^{-1}) = v_p{}^{-1} \qquad (1)$$

in the case of BPF's with the passband bandwidth $(\omega_2 - \omega_1)$ being equal to that of the prototype LPF, or

$$z^{-1} \to (z^{-2} - \alpha z^{-1})/(1 - \alpha z^{-1}) = v_s{}^{-1} \qquad (2)$$

in the case of BSF's with $(\omega_2 - \omega_1)$ (i.e., the region including the transition bands and the stopband of the BSF) equaling $\pi/2 -$ the bandwidth of the LPF. In both cases, α is given by

$$\alpha = \cos[(\omega_2 + \omega_1)/2]/\cos[(\omega_2 - \omega_1)/2] = \cos\omega_0 , \quad (3)$$

where $\omega_0, \omega_1,$ and ω_2 are the center frequency and the lower and upper passband edges, respectively.

Replacing the unit delay elements of a LPF with the transform block, as given by Eq. (1) or (2), has the inherent advantage of reducing the number of multipliers. For example, consider the following second-order section of the prototype LPF with the transfer section

$$H_{lp}(z) = \frac{1 + b_1 z^{-1} + z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \quad . \qquad (4)$$

After using the substitution, as given by Eq. (1) or (2), and realizing the resulting BPF or BSF as a conventional cascade of two second-order sections, six multipliers are required. Alternatively, if each unit delay elements in Eq. (4) is replaced in the direct form II structure by using the transformation blocks given by Eq. (1) or (2), then we would need only five multipliers, as the transformation blocks can be implemented by one multiplier each. For the LPF with zeros not on unit circle, the transformed implementation requires six multipliers compared to eight multipliers required by the conventional cascade of two second-order sections.

Generalizing the low-sensitivity transformations given in [5] we may write the low-sensitivity transformations for BPFs as

$$v_p{}^{-1} = \frac{-(z^{-2} - \alpha z^{-1})}{1 - \alpha(1+k)z^{-1} + kz^{-2}} \qquad (5)$$

and for BSFs as

$$v_s{}^{-1} = \frac{z^{-2} - \alpha z^{-1}}{1 - \alpha(1-k)z^{-1} - kz^{-2}} \ , \qquad (6)$$

where k is a number that can be represented by one bit or at the most two bits in the MNSPT form. Its absolute value is either equal to or less than unity. For example, k may be equal to ± 1, ± 0.5, etc. For most cases, $k = \pm 1$ will suffice.

It can be seen that for $k = 1$ or -1, the transformation given by Eq. (5) is equivalent to Structures *B1* or *B2* for BPFs considered in [5]. Similarly, the transformation given by (6) is equivalent to Structures *B1* or *B2* for BSFs in [5]. The generalized transformation substitution blocks are depicted in Figs. 1 and 2.

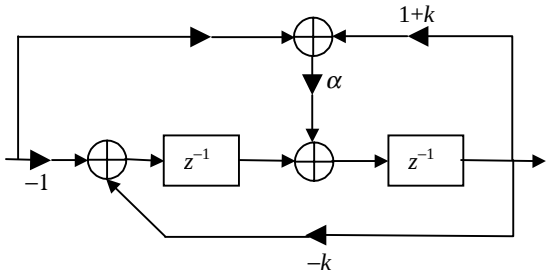

Fig. 1. Transformation block $v_p{}^{-1}$.

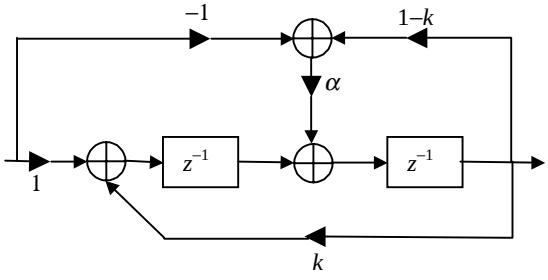

Fig. 2. Transformation block $v_s{}^{-1}$.

For $k = 1$, the modified coefficients for the fourth-order section resulting after transforming from the second-order section, as given by Eq. (4), are expressible as

$$b_{1m}=2+ b_1;\ a_{1m}=2+ a_1;\ a_{2m}=1+ a_1+ a_2 . \qquad (7)$$

In addition, two α–multipliers are needed for the two transformation blocks (those replacing the unit delay elements).

Realization details and the scaling scheme for a fourth-order section (obtained by applying the low-sensitivity transformation to a second-order section of the LPF prototype) are similar to those described in [5; see Fig. 4].

3 RESULTS AND DISCUSSIONS

Quite a few filters were realized in the above manner as cascades of 4th-order sections. Tables 1 and 2 illustrate the results for the implementation for one bandpass filter and one bandstop filter. In both cases, a 12th-order elliptic filter was derived based on a 6th-order elliptic prototype LPF.

The number of nonzero bits required by multiplierless implementations for the original design parameters as well as the resulting slightly increased passband ripples are shown in the tables. In addition, in both cases, a fresh filter was designed using the same method with marginally stricter passband and stopband specifications while keeping the filter order the same. The number of nonzero bits for achieving the original specifications (actually, a slightly smaller passband ripple is obtained) are shown in both cases in the tables.

The dashed and solid lines on Fig. 3 show the amplitude responses for the infinite-precision BPF filter with stricter criteria and for the filter with forty-eight nonzero bits (that is, 3.2 nonzero bits per multiplier on the average).

It is interesting to observe from Fig. 3 that the stopband behaviors of the infinite-precision and finite-precision filters are practically the same. This is mainly due to the fact that we are using a cascade-form realization. For this realization, the effect of coefficient quantization is very small for the zero locations of the overall filter. This is also true for the filters of Tables 1 and 2.

From the above results it is seen that by starting with a filter with revised specification it is possible to implement the multipliers with 3.2 and 3.07 nonzero bits on the average per multiplier for both the BPF and the BSF. Further, it was also seen that by allowing marginal deviations in the bandedges (by reducing the number of nonzero bits for α–multipliers only), an additional reduction in the number of nonzero bits can be achieved. For example, in the case of the BPF, 42 nonzero bits (a reduction of one bit each of the six α–multipliers) leads to the filter with the passband edges being located at 0.1987π and at 0.299π. The corresponding stopband edges are located at 0.1815π and 0.3231π. Similarly, the use of 40 nonzero bits for the multipliers for the BSF leads to a filter with the passband and the stopband edges being located at 0.205π and 0.3545π, and at 0.2227π and 0.3293π, respectively.

Table 1. Requirement of nonzero bits for the example bandpass filter.

Bandpass filter (12th-order) passband edges: 0.2π, 0.3π stopband edges: 0.18π, 0.33π passband ripple: 0.1 dB; stopband attenuation: 50 dB	
Number of nonzero bits for 15 multipliers	Passband tolerances obtained
(a) 77	0.104 dB designed with initial specification
(b) 71	0.121 dB ……”……
(c) 63	0.1275 dB …..”……..
(d) 56	0.1775 dB ……”…….
(e) 48	0.081 dB designed with revised specification of passband ripple of 0.05 dB and stopband attenuation of 51 dB.
Note: Cascade realization of unmodified 4th-order sections needs 20-bit multipliers	

Table 2. Requirement of nonzero bits for the example bandstop filter.

Bandstop filter (12th-order) passband edges: 0.2π, 0.35π stopband edges: 0.22π, 0.32π passband ripple: 0.1 dB; stopband attenuation: 50 dB	
Number of nonzero bits for 15 multipliers	Passband tolerances obtained
(a) 76	0.1009 dB designed with initial specification
(b) 67	0.1045 dB ……”……
(c) 62	0.1068 dB …..”……..
(d) 59	0.1195 dB ……”…….
(e) 56	0.18 dB …..”……
(e) 46	0.095 dB designed with revised specification of passband ripple of 0.05 dB and stopband attenuation of 51 dB.
Note: Cascade realization of unmodified 4th-order sections needs 22-bit multipliers	

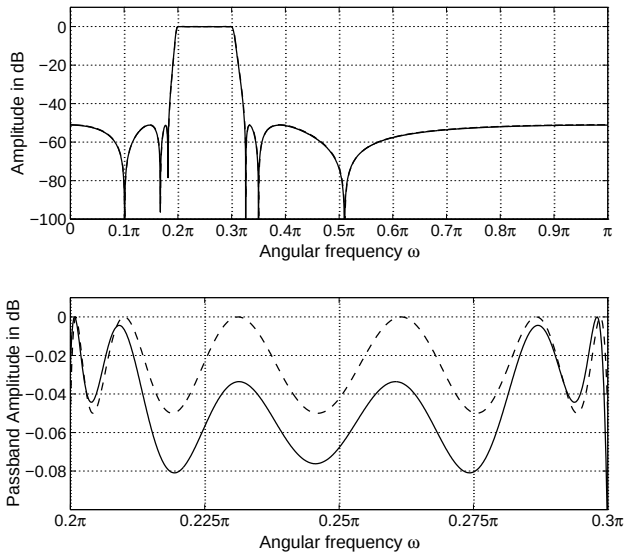

Fig. 3. Amplitude responses for the infinite-precision BPF filter with stricter criteria (dashed line) and for the filter with forty-eight nonzero bits (solid line).

4 CONCLUSIONS

We have shown that the multiplierless implementation of BPFs and BSFs utilizing low-sensitivity transformation structures is a feasible and attractive proposition. Further, considering the acceptance of a marginally small deviation in the passband and stopband tolerance specifications compared to the initial infinite-precision design, the method becomes quite attractive for implementing IIR BPFs and BSFs in the multiplierless manner. Our analysis indicates that utilizing the approach outlined multiplierless realizations can be achieved by using less than four nonzero bits per multiplier on the average without any increase in the filter order. Future work is devoted to applying optimization techniques to further reducing the number of nonzero bits.

5 ACKNOWLEDGEMENT

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