OVERSAMPLING A/D AND D/A CONVERTERS

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ABSTRACT

This tutorial paper explains the principles and areas of application of oversampling data converters. A comparison between Nyquist-rate and oversampling converters is given, and some commonly used architectures discussed for both D/A and A/D oversampling converters.

1. INTRODUCTION

Digital signal processing (DSP) is increasingly becoming the dominant technique for telephony, audio, wireless telecommunications, instrumentation and measurements, and other signal processing applications. Since the input and output signals are typically analog, interface stages containing filters and data converters are needed between the analog signals and the DSP core [1].

In many cases, the A/D and D/A converters needed in the interface can be designed and realized as Nyquist-rate circuits, using sampling rates only slightly higher than twice the bandwidth of the analog signal. However, with the exception of counting-type converters, the accuracy achievable with these circuits is at most 12-14 bits. This is due to the fact that the accuracy is limited by the matching accuracy of the analog components (resistors, or capacitors, or current sources) used in them. Since this is at best around 0.1%, a very high (say 18-bit) accuracy is impractical, even with digital calibration.

Counting converters do not rely on element matching; however, they require a very long time for converting a single sample. For example, the 18-bit conversion of a sample using counting takes 262,144 clock periods. Such low speeds limit the use of counting converters to very-low-frequency (e.g. measurement) applications.

Clearly, there is a large area of applications requiring high accuracy (15-20 bits) and fairly high speed (8 - 500 kS/s) which cannot be met using Nyquist-rate converters. It is this gap which oversampled data converters have been increasingly successful in filling. These converters do not rely on element matching for accuracy; instead, they use a combination of oversampling and noise filtering via feedback to reduce the in-band quantization noise to extremely low levels. The resulting penalty in reduced speed is then much less than for counting converters.

2. DELTA-SIGMA D/A CONVERTERS

Although other oversampled converters (e.g., delta modulator and demodulator) exist, for practical reasons the so-called delta-sigma or noise-shaping converters now dominate the field [2]. The block diagram of a delta-sigma DAC is shown in Fig 1.

The main function of the interpolation filter IF is to increase the sampling rate of the input data from the Nyquist rate f_N to an increased data rate Rf_N, where R is the oversampling ratio. Typically, R ranges from 32 to 1024. IF is also used to suppress the unnecessary spectral replicas centered at f_N, $2f_N$,..., $(R-1)f_N$. Keeping these would reduce the dynamic range of the following NL stage. The design of IF is a challenging task in multi-rate filter design; often the IF is realized by cascaded stages, with each stage clocked at a higher rate than the previous one. Half-band filters seem to be very useful stages of the IF. The word length N_1 at the output of the IF is usually the same as that at its input (N_0), which is also the desired resolution of the conversion, typically 18 - 20 bits.

The next digital block in the system is the noise-shaping loop NL. Its function is to reduce the word length of the signal from N_1 to a much lower value, often to 1, without significantly altering its spectrum inband (i.e., in the signal frequency band). The word-length reduction is necessary for the accurate implementation of the DAC which follows it. A possible implementation of the NL is shown in Fig.2, which contains a truncation block at its output. The preservation of the inband spectrum in spite of this truncation is made possible by the loop filter, which is (for baseband signal conversion) a low-pass filter containing a cascade of accumulators with feedback and feedforward branches. It has a transfer function H(z) with a large gain A(f) over the signal band $0<f<B$. Truncating the output signal of the loop filter to only 1 bit introduces a large error e(n) into the signal path. Since, however, this error is injected after the gain block in the feedback loop, in the z-transform of the output signal the truncation error appears as $E(z)/[H(z)+1]$, and its amplitude

is thus divided by A(f). By appropriate choice of H(z), the energy of the inband error can be reduced to as little as 1 ppm of the signal energy, corresponding to a 20-bit SNR. Assuming that the 1-bit output signal has the values +1/-1, the power of the output signal is fixed. Thus, a reduction of the inband noise in the output signal must be accompanied by a corresponding noise increase out of band. This noise needs to be removed by the analog low-pass filter LPF following the DAC (Fig.1).

The single-bit output data of the noise-shaping loop are converted into a 2-level analog signal by the DAC. Since a 2-level conversion is by definition linear, independent of the elements and reference voltages used (as long as their values are not modulated by the signal), this task can be accomplished in principle ideally - this is the reason for the noise-shaping truncation performed by the NL.

As mentioned above, the large out-of-band noise must be removed from the analog output to achieve the high SNR ratio needed for high-accuracy data conversion. To avoid nonlinear distortion due to slewing of the opamps in the LPF, the major part of the high-frequency noise in the DAC output is first removed by an switched-capacitor (SC) low-pass filter, and the output of this filter is then further smoothed by a continuous-time active (or passive) RC filter to obtain the final analog output signal.

Recently, various techniques were suggested for using a multi-bit, rather than single-bit, DAC in the system of Fig. 1. The motivation for this is that such a system makes the design of both the NL and (more importantly) the LPF much easier. The NL loop is much easier to stabilize if the feedback signal is a multi-bit one, since the equivalent gain of the truncation operation is now well defined. The output of a multi-bit DAC is no longer a two-level signal, but a coarsely quantized replica of the final analog output signal. Its slew rate and high-frequency energy are hence much reduced, which makes it much easier to realize a high-linearity and efficient analog LPF to smooth it.

The problem with the multi-bit DAC system is to insure the linearity of the DAC. Even for very coarse (say, 3- to 5-bit) DACs, the requisite linearity (say, to 18 bits) is impossible to achieve by brute-force matching techniques. Hence, a number of alternative methods have been developed. These include digital calibration [3], error randomization [4], dual truncation [5] and mismatch shaping [6]. In calibration, the error characteristics of the actual DAC are acquired and stored at power-up, and added to the feedback signal in the NL during operation. In error randomization, the DAC is constructed from unit elements, which are randomly chosen during conversion. In dual truncation, there are two truncations performed: one is a single-bit truncation of the signal, the other a multi-bit truncation of the quantization error due to the 1-bit truncation. Now the nonlinearity of the second truncation does not contribute to the harmonic distortion of the signal.

The latest technique for linearizing multi-bit DACs is mismatch shaping. In this method, the error signal due to DAC nonlinearity is high-pass filtered, much as the truncation noise is in the NL. This requires additional digital circuitry, which however remains reasonably simple if the resolution of the internal DAC is low (3 to 6) and the order of the shaping function is only 1 or 2.

3. DELTA-SIGMA A/D CONVERTERS

The operation of delta-sigma ADCs is also based on oversampling, noise shaping and filtering. The block diagram is illustrated in Fig.3. It contains only a noise-shaping loop NL and a digital decimation filter DF. Now the input signal is analog, and it is directly sampled at an oversampled rate into an analog NL of the form shown in Fig.4. The loop is similar to that shown in Fig.2. However, it contains a 1-bit ADC (usually simply a latched comparator) instead of the 1-bit truncator, and it also needs a 1-bit DAC in its feedback path. The loop filter is a sampled-data analog one, usually realized as a cascade of switched-capacitor integrators, with feedback and feedforward branches added [2]. The NL is followed by a digital decimation filter DF which transforms the oversampled single-bit output data of the NL into the final Nyquist-rate multibit output signal of the ADC. The noise shaping is again performed by the high-pass filter function 1/[H(z)+1], which is insensitive to the inaccuracies of the analog elements of the NL.

An alternative NL architecture, called a cascade or MASH system, is shown in Fig.5 [7]. This system contains two oversampling NLs; the upper one is used to convert the signal, and the lower one to convert the quantization error of the upper loop, into digital signals. These are then combined to cancel the quantization error of the upper loop. The MASH structure also provides noise shaping for the quantization error of the second NL. This error is filtered by approximately 1/[H1.H2], where H1 is the transfer function of the upper loop filter, and H2 is that of the lower one. The stability of the system is determined by the two loops operating separately, and hence a high-order (say, 4th-order) noise shaping is possible with the more robust stability of a lower-order (second-order) loop, if two second-order loops are combined in the MASH structure. Also, it is possible to use multi-bit quantization in the second loop without introducing nonlinear signal distortion [2].

The DF can be a single high-order FIR low-pass filter, which takes advantage of the single-bit nature of the NL output data to avoid any multiplications. More often, it is realized in the form of cascaded stages with decreasing sampling rates. The first few stages are usually sinc^K filters, followed by more conventional half-band FIR structures [2].

Again, the stability of the NL is much improved, and the design of the DF simplified, if the internal ADC and DAC

have higher than single-bit resolution. The methods briefly described for multibit DACs in the previous Section remain applicable in this context as well.

4. ACKNOWLEDGMENTS

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5. REFERENCES

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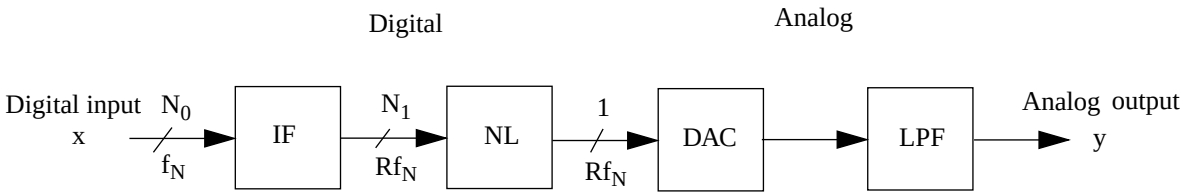

IF: Interpolation filter
NL: Noise shaping loop
DAC: D/A converter
LPF: analog low-pass filter

Figure 1. Block diagram of a ΔΣ DAC

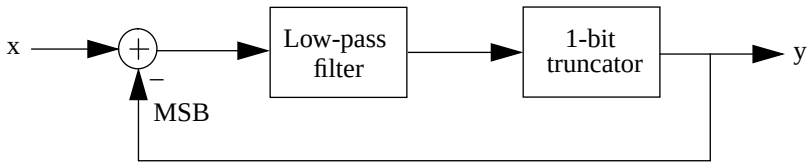

Figure 2. General block diagram for a ΔΣ noise-shaping loop

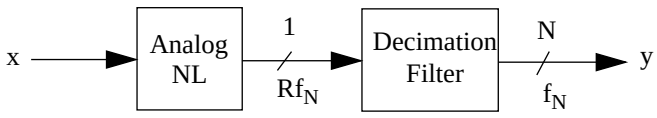

Figure 3. Block diagram of a ΔΣ ADC

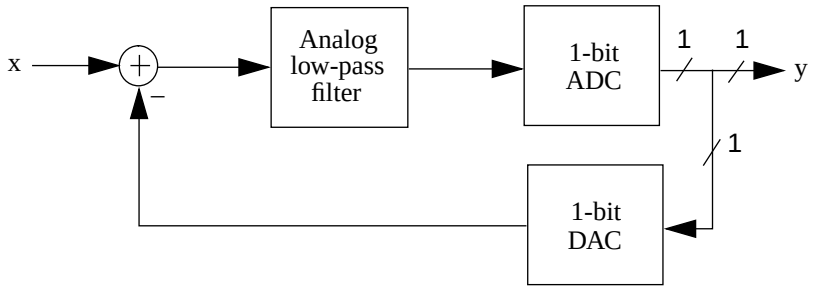

Figure 4. An analog noise shaping loop

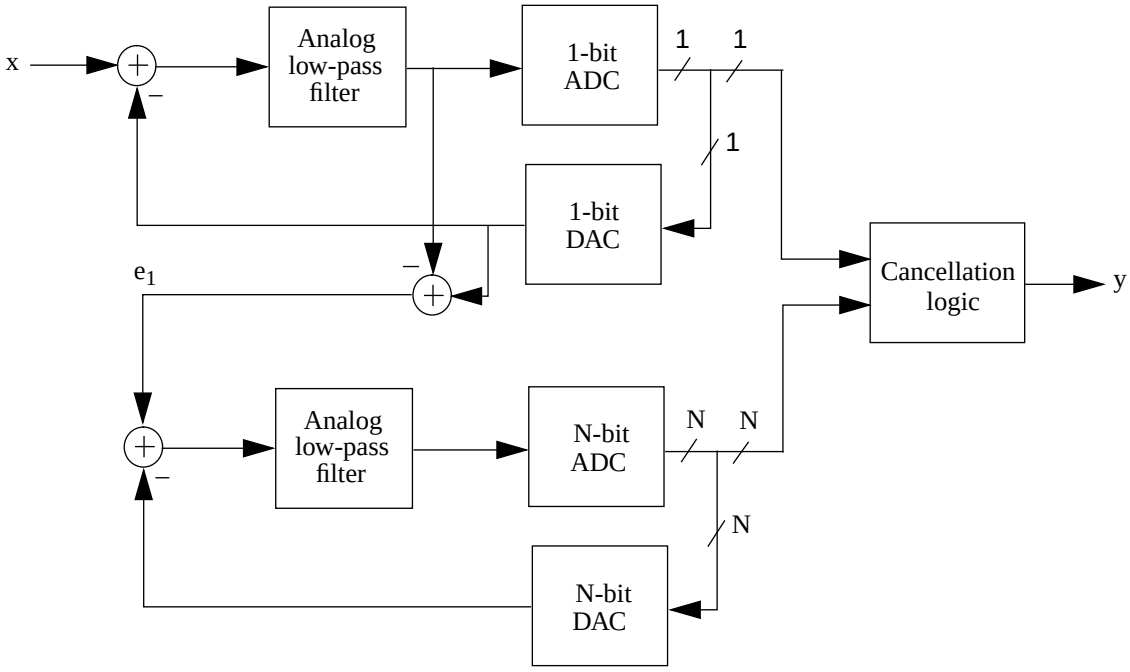

Figure 5. A cascaded ΔΣ modulator