ALGORITHMIC NOISE-TOLERANCE FOR LOW-POWER SIGNAL PROCESSING IN THE DEEP SUBMICRON ERA

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ABSTRACT

In deep submicron (DSM) VLSI technology, deviations in node voltages due to DSM noise can lead to erroneous system outputs in VLSI implementations of DSP and communication algorithms degrading their performance in terms of signal-to-noise ratio (SNR) or bit-error-rate (BER). We present algorithmic noise-tolerance schemes for digital filtering to detect such errors in system output and mitigate their effect on the system performance. The errors in the system output are detected by employing a low-complexity prediction scheme. It is shown that, the proposed scheme improves the performance of the filtering algorithm by up to 10dB with less than 10% hardware overhead. It is also shown that the proposed scheme can be employed to achieve substantial energy savings with marginal degradation in performance by deliberately introducing errors in DSP hardware by *overscaling* the supply voltage.

1 INTRODUCTION

It is now well established [1] that, in deep submicron(DSM) technology, phenomena such as ground bounce, cross-talk, process parameter variations, charge sharing, charge leakage, and slow and unpredictable interconnects lead to deviations in node voltages from their nominal values of 0 and V_{dd}. These deviations are commonly referred to as *DSM noise*. Recent proposals to tackle the problem of DSM noise range from interconnect centric design methodologies [2] and re-characterization of devices and interconnect for future process generations to systematic static noise analysis methodology [1] to locate nodes where large deviations in voltage could occur.

As a complement (and perhaps an alternative) to noise reduction/analysis [2, 1], we propose the notion of *algorithmic noise tolerance* (ANT) for combating DSM noise. The noise tolerance (as opposed to noise elimination) approach involves providing adequate amount of noise immunity based on the level of reliability demanded by the application. This approach is well suited for VLSI implementations of DSP and communications algorithms as the performance of these algorithms is specified in terms of average metrics such as signal-to-noise ratio (SNR) and bit-error-rate (BER).

Reliability issues related to signal processing and communication algorithm implementations have been addressed in the past. A general purpose algorithm based fault tolerance (ABFT) scheme for matrix multiplication operation was proposed in [7] and employed for DSP algorithms by reducing them to a set of basic matrix operations. In [8], an error detection scheme for the filtering operation was developed via polynomial residue codes in large finite integer rings. A fault tolerant adaptive filtering algorithm was proposed in [9] wherein, hardware redundancy is employed to provide fault tolerance. Note that these scheme do not exploit the signal statistics and energy-efficiency is not a concern in these works.

Recently, it has been established [10] that energy dissipation can be traded off for reliable operation in DSP systems by *overscaling* the supply voltage. The proposed ANT schemes can then be employed to restore the degradation in algorithmic performance due to input dependent errors that occur as a result of overscaling. In this paper, we present the performance of the proposed ANT schemes in restoring the performance degradation in both the scenarios.

The rest of this paper is organized as follows. In section 2, we illustrate how voltage deviations at the circuit level can lead to degradation in DSP system performance through a simple example. In section 3, we present the ANT schemes that can be employed to restore performance degradation in digital filters due to either DSM noise or voltage overscaling. Simulation results are presented in Section 4 and conclusions and possible future research directions are discussed in Section 6.

2 IMPACT OF DSM NOISE ON DSP SYSTEM PERFORMANCE

Consider the dynamic CMOS inverter [11] shown in Figure 1(a), in which, during the evaluate phase, V_{out} should stay high if $V_{in} = 0$. However, as shown in the voltage waveforms in Figure 1(a), a positive glitch with

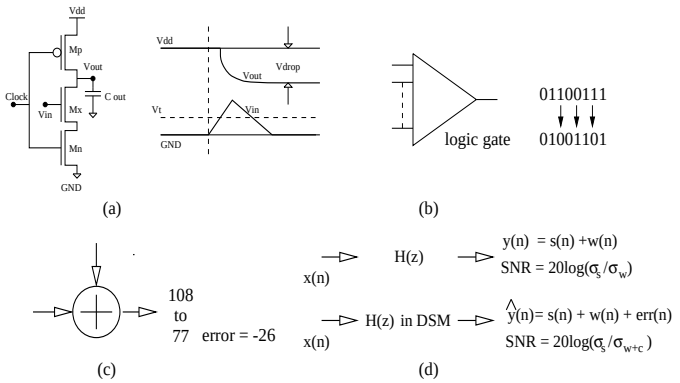

Figure 1: DSM noise: (a)circuit level voltage deviations, (b) errors induced at the logic level, (c) numerical errors at the architectural level, and (d) system level performance degradation.

amplitude more than the threshold voltage V_t of M_x and of sufficiently long duration can cause a drop in V_{out} that can be high enough to cause a logical error. Though *dynamic logic* is an attractive circuit style [11] in terms of speed, area, and power, as shown in Figure 1(a), it is susceptible to voltage deviations due to *ground bounce*, *charge sharing*, *charge leakage* etc.

When the voltage deviations at the circuit level are substantial in magnitude and duration, they lead to logical errors at the logic level as shown in Figure 1(b). In this case, 3 bits in the 8-bit output have flipped due to DSM noise. At the architectural level, the effect of voltage deviations depend on the functionality of the architectural blocks. Hence, if the gate in Figure 1(b) were an adder as shown in Figure 1(c), the numerical value of the error would be -26 assuming that 2's complement number representation is employed. The impact of numerical errors at the architectural level on the DSP algorithm performance is illustrated in Figure 1(d). In the absence of DSM noise, the performance of the filter transfer function $H(z)$ is measured in terms of the output SNR given by

$$SNR = 20\log(\sigma_s/\sigma_w), \tag{1}$$

where σ_s is the signal power and σ_w is the signal noise power, i.e.,

$$y(n) = s(n) + w(n), \tag{2}$$

where $s(n)$ is the desired signal and $w(n)$ is the signal noise. In presence of DSM noise, we have,

$$\hat{y}(n) = y(n) + err(n), \tag{3}$$

where $err(n)$ is the error introduced due to DSM noise and,

$$SNR = 20\log(\sigma_s/(\sigma_{w+c}), \tag{4}$$

where σ_{w+c} is the total noise power that includes signal and DSM noise. The goal of ANT is to achieve a value

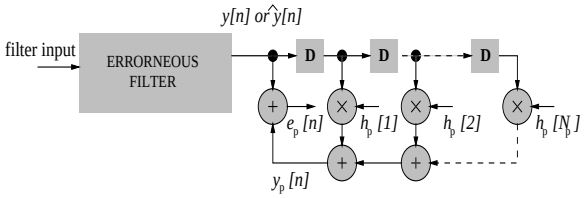

Figure 2: Prediction-based algorithmic noise-tolerance scheme

of σ_{w+c} that is as close to σ_w as possible via system level error control.

Note that the degradation in SNR depends on the noise power σ_{w+c}. Hence, in general, the amount of protection necessary is dependent on the performance demands of the particular application.

3 Algorithmic Noise Tolerance

The error-control algorithm presented in [10] is based on linear prediction [12]. In this section we present a brief review of these algorithms.

The output of a digital FIR filter shown in Fig. (2), when the filter is error-free, is denoted by $y[n]$ and is given by,

$$y[n] = \sum_{k=0}^{N-1} h[k]x[n-k], \tag{5}$$

where $h[k]$ denotes the filter impulse response, $x[n]$ is the filter input and N is the number of taps in the filter. Let $\hat{y}[n]$ denote the filter output when the filter is operating under reduced voltage, with $\hat{y}[n] = y[n] + y_{err}[n]$, where $y_{err}[n]$ denotes the error in the filter output due to soft errors. Note that $y_{err}[n]$ is non-zero only when the input pattern is such that longer paths in the filter implementation are excited. Let $y_p[n]$ denote the output of an N_p-tap predictor when the filter is noiseless, i.e.,

$$y_p(n) = \sum_{k=0}^{N_p} h_p[k]y[n-k], \tag{6}$$

where $h_p[k]$ denotes the *optimum predictor coefficients* [12] that minimize the mean squared value (MSE) $< e_p^2[n] >$ of the prediction error $e_p[n]$, given by,

$$e_p[n] = y[n] - y_p[n]. \tag{7}$$

The minimum mean square error (MMSE) depends on the autocorrelation function of $y[n]$ and the order of the predictor. Let $\hat{y}[n]$, $\hat{y_p}[n]$, and $\hat{e_p}[n]$ denote the filter output, the predictor output, and the prediction error, respectively, in presence of soft errors. It can be shown that

$$\hat{e_p}[n] = y_{err}[n] + e_p[n]. \tag{8}$$

Assuming that no more errors occur in the next N_p output samples, we can show that,

$$\hat{e_p}[n+m] = -h_p[m]y_{err}[n] + e_p[n+m], \tag{9}$$

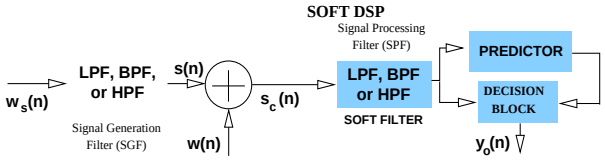

Figure 3: Simulation setup to evaluate the proposed scheme.

for $m = 1, \cdots, N_p$.

The error-control algorithm presented in [10] is based on the fact that, in absence of errors, the magnitude of the prediction error is small and is inversely proportional to the correlation in the digital filter output. In presence of a soft error, the magnitude of the prediction error increases substantially and the erroneous sample leads to errors in the subsequent output samples of the predictor. Hence a pattern of errors is generated. This pattern is exploited to detect errors in the filter output. In case an error is detected, the predictor output corresponding to the erroneous sample is resolved to be the actual filter output.

The effectiveness of this scheme depends on the following factors:

- **output correlation:** The correlation in the filter output determines the accuracy of the predictor. Hence, for highly correlated outputs such as narrowband filters, the prediction error is extremely small in absence of errors. Hence the probability of detecting an error with a large amplitude increases.

- **error frequency:** In case of DSM noise, the error frequency is dependent on several factors such as technology, physical design etc. In case of voltage overscaling however, the frequency of errors depends on the factor by which the supply voltage has been scaled and, more importantly, on the delay imbalance present in the architecture employed.

In the next section, the performance of the error detection and correction schemes described above are simulated in the scenario where a digital filter is employed to reduce out-of-band noise in a band pass signal. It is also shown that the proposed approach provides for substantial reduction in energy dissipation with marginal performance degradation.

4 EXPERIMENTAL RESULTS

The setup used to measure the performance of the proposed scheme in which the filtering algorithm is employed in the frequency selective filtering configuration is shown in Figure 3. A lowpass, bandpass or a highpass filter (LPF, BPF or HPF), denoted as the signal generation filter (SGF), is used to generate a bandlimited signal $s(n)$ from a wideband input $w_s(n)$. The signal $s(n)$ is the corrupted by wideband noise $w(n)$, i.e., the signal

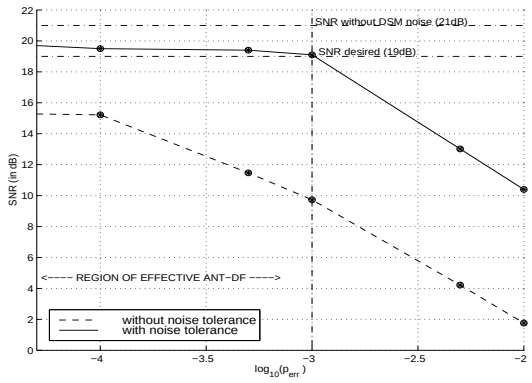

Figure 4: Performance of the proposed ANT scheme for filter bandwidth $\omega_b = 0.2\pi$ with predictor tap-length, $N_p = 2$.

$s_c(n)$ is obtained as $s_c(n) = s(n) + w(n)$, where $s(n)$ is the output of the SGF for a wideband input $w_s(n)$. As $s(n)$ is bandlimited, the SNR can be improved by passing $s_c(n)$ though a frequency selective filter with bandwidth ω_b. This filter is denoted as the signal processing filter (SPF) in Figure 3, and it supresses the out-of-band components of the noise signal $w(n)$.

4.1 Performance Measures

The SNR at the output of the filter in presence of errors is given by,

$$S\hat{N}R_o = 20\log_{10}\left(\frac{\sigma_s}{\sigma_n + \sigma_c}\right), \qquad (10)$$

where σ_s^2 is the variance of the signal component (due to $s(n)$), σ_n^2 is the variance of the noise component (due to $w(n)$),and σ_c^2 is the variance of error in the output due to voltage overscaling or DSM noise (i.e., $< y_{err}(n)^2 >$).

4.2 Performance of ANT in the Presence of DSM Noise

In order to experimentally verify the effectiveness of the proposed approach in presence of DSM noise, errors are introduced at the system level by flipping the output bits of the digital filter independently, with a fixed probability denoted by p_{err}. Note that more accurate performance results require detailed DSM noise models for the arithmetic units employed in the digital filter which are currently not available. The performance of the proposed algorithm for a digital filter with bandwidth $\omega_b = 0.2\pi$ and 48 taps is shown in Figure 4. As expected, without noise-tolerance, the degradation in performance increases with increase in p_{err} as expected. Also, the proposed scheme provides up to $10dB$ improvement in performance. The SNR with ANT stays almost constant above $19dB$ till $p_{err} = 10^{-3}$ and then reduces sharply. In this range, the probability of error is low enough that the assumption of infrequent errors (assumption 2 in section 3.3) is satisfied. Hence,

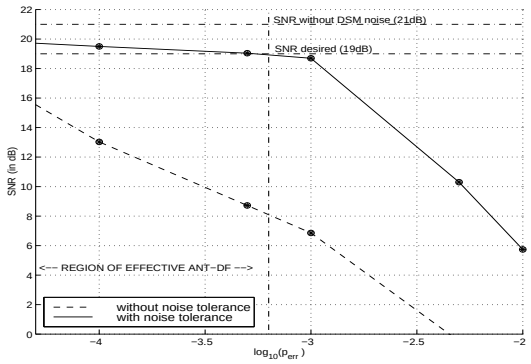

Figure 5: Performance of the proposed ANT scheme for filter bandwidth $\omega_b = 0.4\pi$ with predictor tap-length, $N_p = 4$.

error detection is performed effectively. As p_{err} is increased, this assumption is not satisfied any more and hence there is a rapid degradation in performance of the proposed algorithm. Similar results for a bandwidth of $\omega_b = 0.4\pi$ are shown in Figure 5. Note that in both the cases, the proposed scheme is quite effective in combating DSM noise that is large enough to cause bit-errors at a rate of 1 per 1000 samples.

4.3 Performance of ANT for voltage overscaling

The plot of energy-savings due to voltage overscaling vs. algorithmic performance for the above implementation for a filter of bandwidth $\omega_b = 0.2\pi$ is shown in Fig. 6. The reduction in energy dissipation has been obtained via HSPICE from an implementation of the proposed ANT scheme that is currently under fabrication. The algorithmic impact of voltage overscaling were obtained using a high-level delay simulator similar to the one employed in [10]. Note that upto 76% reduction in energy dissipation is possible with a penalty of less than $1dB$ in algorithmic performance.

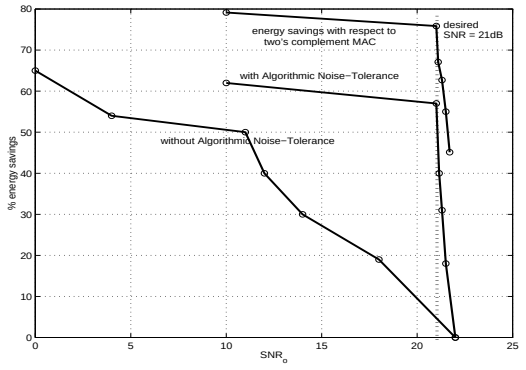

Figure 6: energy-dissipation vs. algorithmic performance for the proposed implementation

5 Conclusion

In this paper we have discussed a novel approach that can be employed effectively as a low-power technique in presence of DSM noise in future technologies for DSP and communications applications. Future work on this topic will involve development of error-control schemes for widely used DSP algorithms such as lattice, IIR, and adaptive filtering etc., and applications such as as wireless communications where energy-efficiency is a primary concern.

References

[1] K. L. Shepard "Conquering Noise in Deep-Submicron Digital ICs," *IEEE Design and Test of Computers*, Jan-Mar 98, pp. 51-62.

[2] P. J. Restle et. al. "Interconnect in high speed designs: problems, methodologies and tools," *ICCAD 98,* San Jose, CA.

[3] The 1997 National Semiconductor Technology Roadmap, *URL: http://www.sematech.org.*

[4] A. Chandrakasan and R. W. Brodersen, "Minimizing power consumption in digital CMOS circuits," *Proceedings of the IEEE*, vol. 83, no. 4, pp. 498-523, April 1995.

[5] J. D. Meindl, "Low power microelectronics: Retrospect and prospect," *Proceedings of IEEE*, vol. 83, no. 4, pp. 619-635, April 1995.

[6] E. A. Vittoz, "Low-power design: Ways to approach the limits," *ISSCC '94*, pp. 14-18, San Fransisco, CA.

[7] J.-Y. Jou and J. A. Abraham, "Fault-tolerant matrix arithmatic and signal processing on highly concurrent computing structures," *proceedings of the IEEE,* pp. 732-741, May 1986.

[8] G. R. Redinbo, "System level reliability in convolution computations," *IEEE trans. ASSP,* pp. 1241–1252, Aug. 1989.

[9] B. A. Schnaufer and W. K. Jenkins, "Adaptive Fault Tolerance for Reliable LMS Adaptive Filtering," *IEEE Trans. on Circuits and Systems, Part II,* vol. 44. no. 12. pp 1001-1013, Dec. 1997.

[10] R. Hegde and N. R. Shanbhag, "Energy-efficient signal processing via algorithmic noise-tolerance," *Proceedings of 1999 ISLPED,* pp. 30-35, August, 1999.

[11] J. M. Rabaey, *Digital Integrated Circuits: A Design Perspective.* Prentice-Hall, New Jersey, 1996.

[12] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing: Principles, Algorithms and Applications* Prentice-Hall, New Jersey, 1996.