REAL-TIME FPGA IMPLEMENTATION AND MEASURED PERFORMANCE OF I/Q MODULATION BASED FREQUENCY SYNTHESIZER

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ABSTRACT

In this article, the design and implementation of mixed-signal frequency synthesis for wireless communications devices are addressed. The core of the synthesizer builds on digitally synthesized tunable low-frequency I/Q tone which is then shifted to the actual radio frequency range using I/Q modulation. An efficient real-time FPGA design of the digital synthesizer core is first provided. This is then also implemented in real time and connected to practical I/Q modulation hardware to measure the spectral characteristics of the overall synthesizer, in terms of phase noise and spurious frequencies. Specific emphasis in the implementation structure is on adaptive digital pre-distortion and calibration mechanisms that improve the limited sideband attenuation and local oscillator leakage of practical I/Q modulators. Measured results indicate that the reported design of the proposed architecture can provide more than 50dB spurious free dynamic range at the final synthesizer output.

Index Terms — *Frequency synthesis, spurious components, digital pre-distortion, I/Q modulation, FPGA's, prototype implementation, signal processing systems*

1. INTRODUCTION

Frequency synthesis is a fundamental part of any radio device. Oscillating signals are needed to shift signals between radio frequencies (RF), intermediate frequencies (IF), and baseband frequencies [1]-[5]. Frequency synthesis performance is typically a compromise between switching speed, phase-noise characteristics, frequency range and spectral purity [4].

At implementation level, phase locked loop (PLL) based synthesizers are most often used but for systems requiring very fast switching time, like frequency hopping radios, providing sufficient phase noise behavior with analog PLL structures can be challenging [1], [2], [4]. A direct digital synthesizer (DDS), in turn, has very fast switching time but the usable frequency range is not sufficient for most radio frequencies being in the GHz range [3]. Combining a DDS with an I/Q modulator, as originally proposed in [6], [7], and illustrated in Fig. 1, is conceptually an interesting alternative, but practical circuit limitations especially on the I/Q modulator side can easily limit the spectral purity. This includes, e.g., the achievable suppression of the local oscillator (LO) leakage and mirror frequency components at the overall synthesizer output. Best analog I/Q modulators provide typically only 25-40 dB attenuation for these components, if no additional signal processing is deployed [8],[9], which is insufficient.

This article focuses on both the actual hardware implementation as well as the needed calibration signal processing of the I/Q modulator based synthesizer illustrated at conceptual level in Fig. 1. First simple yet efficient mechanisms to estimate digital calibration parameters for enhancing the LO suppression and mirror frequency attenuation are described. Then the operation and performance of the synthesizer are emulated in floating point simulation domain. After this, to study the performance and limitations of the overall synthesizer in real time, a fixed point implementation is provided, together with simulation verifications and analysis. This is then followed by a register transfer level (RTL) implementation, which is connected to I/Q modulation hardware to actually measure the operation and performance of the overall synthesizer architecture in real-time conditions.

In terms of tools and implementation platforms, Matlab/Simulink with Xilinx System Generator FPGA development tool is used for all the development work. The simulation system uses general floating point Simulink blocks for the testbench features and the parts not specifically targeted for the FPGA. This reduces the development work and simulation times significantly and the focus can then be on the RTL implementation. The FPGA implementation itself can use System Generator library components, standard IP block from Xilinx or hand written very large scale integrated circuit (VLSI) hardware description language (VHDL). The I/Q modulator, in turn, is built using commercial off-the-shelf discrete components, in order to have a versatile and easily configurable prototyping system.

2. SYNTHESIZER ARCHITECTURE

Like shortly described already in Section 1, the basic idea to synthesize a fast tunable RF tone is to combine direct digital synthesis and I/Q modulation. As illustrated in Fig. 1, the DDS part provides the frequency tuning in terms of tunable low-frequency tone(s) in I/Q form. These I and Q tones, when connected to an I/Q modulator, form the final synthesizer output at desired radio frequencies. In fast frequency hopping applications, the analog LO feeding the I/Q modulator can run at fixed frequency and all the tuning is done using the DDS. Completely different center-frequency ranges, however, demand corresponding changes also in the analog LO frequency due to limitations in the DDS frequency range.

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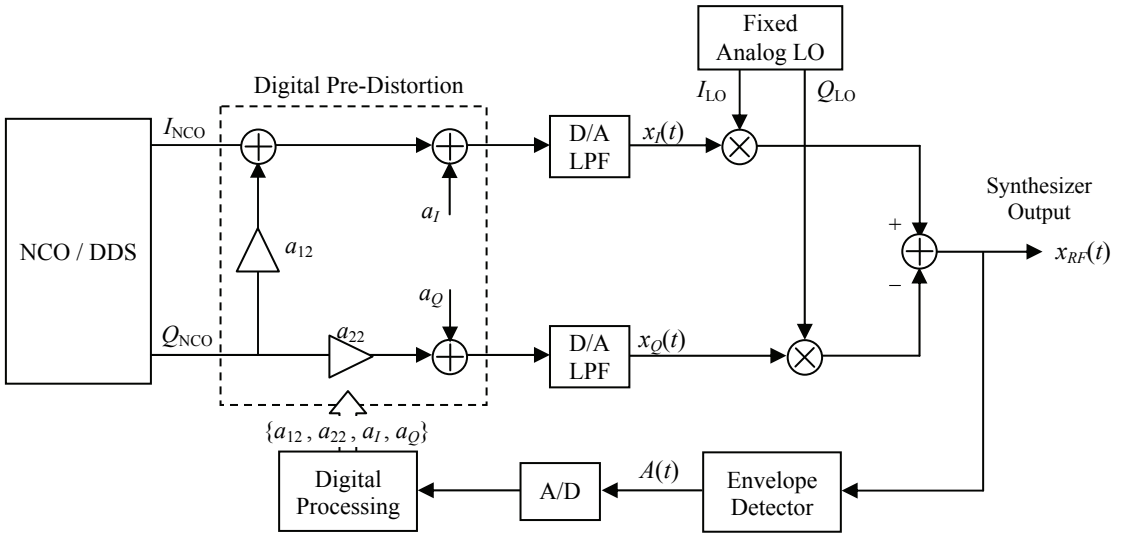

Fig. 1. Principal synthesizer architecture where direct digital synthesis (DDS) is combined with I/Q modulation. Digital pre-distortion is used to compensate for the non-idealities of the analog part whose parameters are estimated using output envelope feedback.

Some of the biggest implementation problems in the above architecture are circuit nonidealities in the analog I/Q modulator. This includes limited isolation between the mixer LO and RF ports and finite attenuation for the mirror frequency component due to I and Q branch amplitude and phase differences, both leading to spurious components at the synthesizer output [8], [9]. Without any additional calibration mechanisms, state-of-the-art I/Q modulators yield typically only 25-40dB attenuation for the LO leakage and mirror frequency component, relative to the desired frequency at the output [10]-[12].

Such I/Q modulator impairment correction is actually fairly widely studied and many alternative techniques have been proposed, see, e.g., [10]-[12]. These are, however, mainly targeted for I/Q modulators in data communication and not for frequency synthesis as such. Therefore most reference works are dealing with a more complicated subject and are computationally more complex than the solution suggested initially in [7] for synthesizer calibration. This method uses only the envelope of the synthesizer output, and is used as the baseline also in this article. The actual signal processing, as illustrated in Fig. 1, relies on four predistortion coefficients, a_{12}, a_{22}, a_I and a_Q which are used to pre-distort the DDS I and Q components such that the LO leakage and mirror-frequency component at synthesizer output are suppressed. For complete signal modeling and derivations of the optimum coefficients with known impairments, refer to [7].

In practice, the exact impairment levels are, however, unknown and can also change, e.g., as a function of the operating temperature. To emphasize implementation simplicity, the predistortion parameter estimation relies here only on the *envelope variation* of the synthesizer output. This is stemming from the fact that under ideal operation, a constant envelope RF tone is obtained, while any spurious components are generally creating amplitude modulation. Here the idea is to use the current envelope variation as a relative measure to update the pre-distortion coefficients. Also, if update is done for only one parameter at a time, monitoring how the envelope variation reacts to parameter update (increases or decreases) gives information whether the update direction was successful or not, given that the update step-size reasonably small. This can in principle be seen as one-dimensional gradient rule, separately for each parameter, and can be formulated at principal level as

$$a_x(n) = a_x(n-4) + K_x(n)\lambda_x dA_x(n) \qquad (1)$$

In above, a_x refers to any of the pre-distortion parameters a_{12}, a_{22}, a_I and a_Q at a time, and λ_x is the adaptation step-size for parameter a_x. Furthermore, dA_x denotes the current envelope variation obtained through the feedback path, and the parameter K_x is the sign parameter which controls the direction of the adaptation. This is obtained as $K_x(n) = +K_x(n-4)$ or $K_x(n) = -K_x(n-4)$, depending whether the previous update of a_x (at time instant $n-4$) caused the envelope variation dA_x to decrease or increase. Notice that computationally more challenging adaptation rules are described in [6]-[7] but here the above simple feedback adaptation rule is proposed and demonstrated in the following sections through actual radio signal measurements and real-time hardware to provide an efficient solution. The proposed update rule in (1) is also highly computationally efficient for real-time implementations.

3. FPGA IMPLEMENTATION

3.1 Design Environment and Tools

The implementation and simulations in this article are carried out using the Xilinx System Generator tool. The implementation is targeted for Virtex-II FPGA technology and synthesis is done using Xilinx XST while place and route (PAR) is done using Xilinx ISE. Real time measurements are carried out using the XtremeDSP Kit from Xilinx. The XtremeDSP board consists of a Virtex-II FPGA, D/A converters and A/D converters needed for the system implementation [13].

System Generator is an additional block-set for Matlab/Simulink graphical design environment that uses Xilinx IP blocks. The simulation speed is significantly faster than RTL-simulators and the tight integration to Matlab makes test signal generation and analysis of results quite convenient. Selected

parts of the simulation model can be in floating point domain and implemented using Simulink blocks or M-code. Only the components targeted for the FPGA implementation are implemented in fixed point domain using System Generator blocks. This feature is very important when modeling systems with feedback from analog parts, and allows e.g. efficient modeling of RF sections in the overall simulation flow.

3.2 FPGA Architecture

For the design and simulations, a low-pass equivalent model of the analog RF parts is used. The overall simulation model block diagram is illustrated in Fig. 2. The low-pass equivalent of the synthesizer output is calculated directly from the pre-distorter coefficients and baseband equivalent model of the analog RF parts, including the imperfection models, in floating point domain. The envelope signal is then quantized in the GW-in block to 14-bit fixed point format. GW-out blocks, in turn, are used to convert the coefficient values to floating point format.

The functionality of the block 'Digital Processing', seen in Fig. 1, is divided into two components, namely 'dA' and 'Control'. The difference of the envelope maximum and minimum values is calculated in block 'dA' over the period of the coefficient update cycle. The output data width of the block 'dA' was set to 15-bits to maintain adequate precision. The block 'Control', in turn, updates one of the pre-distortion coefficients for each dA value in periodic manner, based on the update rule (1). Coefficient bit width used for 'Control' block output was here 16-bits, since it was observed that bit widths longer than this do not provide any improvement in performance. In the simulations, on the other hand, increasing the envelope feedback path A/D-converter precision and the digital processing data widths results in almost linear improvement of 5 dB/Bit in the calibration performance which is here measured by the achieved suppression of the LO-leakage and mirror frequency components at the overall synthesizer output after pre-distorter convergence.

The behavior of the adaptation system can be best observed by monitoring the envelope variation rate *dA,* illustrated in Fig. 3. In this example, the analog I/Q modulator imperfection parameters are: I/Q gain error = 4 %, I/Q phase error = 6 degrees, I/Q delay error = 1degree, I-branch LO leakage attenuation = 40 dB and Q-branch LO leakage attenuation = 35 dB. These represent realistic example numbers, and result in the overall LO leakage of around 30 dBc and mirror tone attenuation of 28 dBc at the synthesizer output without additional calibration (pre-distortion). As seen in Fig. 3, the behavior of the fixed point RTL implementation is almost identical to the ideal floating point model. At start-up, it takes the RTL system some update cycles to get proper values loaded to all registers. This can be seen as small delay in convergence. The convergence of the actual pre-distorter coefficients in this example is presented in Fig. 4 and Fig. 5.

The corresponding spectrum of the low-pass equivalent synthesizer output after pre-distorter convergence in this example is shown in Fig. 6. Here the LO leakage appears at zero frequency while the mirror tone is at the mirror frequency compared to the main tone around origin. The obtained overall attenuation levels for the LO leakage and mirror tone are 73dBc and 82dBc, respectively. This corresponds to improvements of 73-30 = 43dB and 82-28 = 54dB, respectively. This already demonstrates that the effects of the proposed simplified update rule (compared to [7]) as well as the effects of finite word length, used for the fixed-point implementation, are well controlled, and the quality of the synthesizer output in terms of spurious component attenuation is very good.

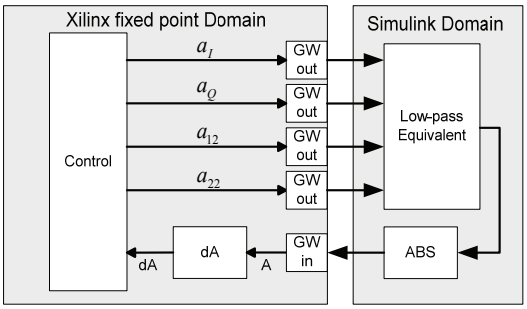

Fig. 2. Principal co-simulation model.

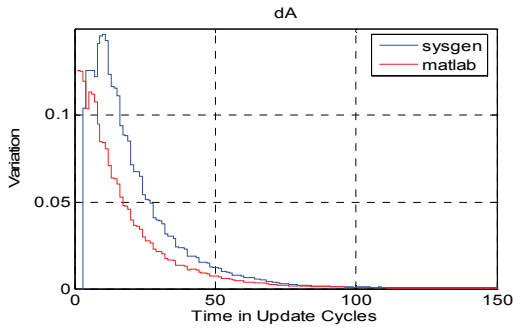

Fig. 3. Output envelope variation behavior during pre-distorter adapation.

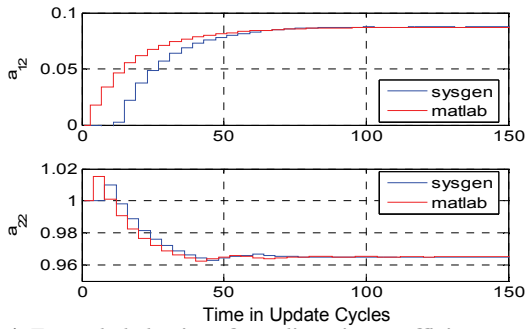

Fig. 4. Example behavior of pre-distortion coefficients a_{12} and a_{22} during the adaptation.

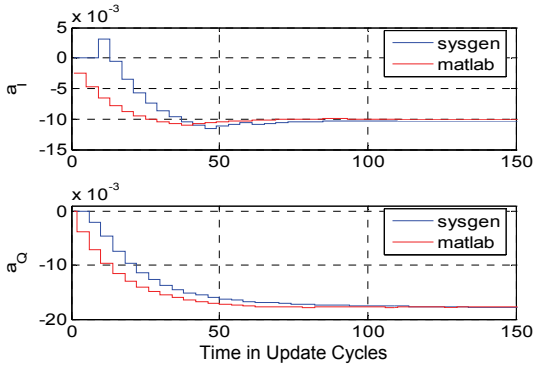

Fig. 5. Example behavior of the pre-distortion coefficients a_I and a_Q during the adaptation.

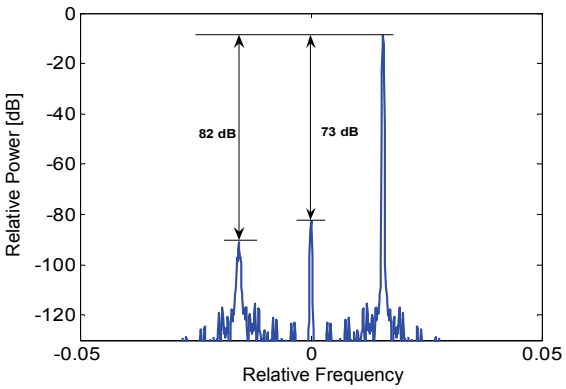

Fig. 6. Low-pass equivalent output spectrum of the whole synthesizer after pre-distorter convergence.

In general, the digital part of the synthesizer architecture is not costly to implement. The usage of Virtex-II FPGA resources is shown in Table 1. The logic utilization is reported in slices. In Virtex-II architecture, a slice contains two 4-input LUTs and two D-type flip-flops when used for logic. The total Slice usage of 923 is only 16% of the XC2V3000 FPGA used in the XtremeDSP Kit [13]. The coefficient update block named 'Control' is the largest component and has been implemented using four identical blocks in parallel configuration, one for each coefficient. Since only one coefficient is actually updated at a time, a time-shared architecture could be used to further lower the resource utilization in practice.

4. MEASUREMENT RESULTS

4.1 Measurement System

An overall block-diagram of the RF measurement set-up is depicted in Fig 7. The analog I/Q modulator was implemented using discrete components from Mini-Circuits and a laboratory signal generator is used as the LO signal generator. As an illustrative example, the DDS output frequency was selected to be -0.5 MHz and the analog LO frequency was set to 100 MHz. Thus under ideal conditions, the overall synthesizer output should contain a single RF tone at 100 MHz - 0.5 MHz = 99.5 MHz. As the feedback path envelope detector, an I/Q demodulator evaluation board and discrete low-pass filters, with cut-off frequency of 10.7 MHz were used to down-convert the synthesizer output signal to a low-IF frequency of 9 MHz. These I and Q signals are then sampled at IF and digitized with 14-bit A/D converters, and the envelope is calculated from the sampled I and Q components on the digital hardware.

The block diagram of the digital part of the measurement set-up can, in turn, be seen in Fig. 8. In the feed-forward I and Q signal paths, the digital output signal is right-shifted three times before D/A conversion to reduce harmonic distortion. In the feedback signal loop, in turn, digital down-conversion and absolute-square operations are used to calculate the envelope feedback signal, stemming from the use of I/Q demodulator hardware and IF sampling in the analog feedback part.

4.2 Results

The spectrum of the complex digital feedback signal after digital down-conversion, yet without pre-distortion, can be seen in Fig 9. The desired tone is located at +0.5 MHz, LO leakage term can be seen at zero frequency and the mirror-frequency component caused by I/Q-imbalance is at -0.5 MHz. The envelope signal is formed from this signal in time domain by calculating the sum of absolute squares of the underlying I and Q components.

The actual measured synthesizer output spectrum without pre-distortion is illustrated in Fig. 10. The desired tone is at 99.5 MHz while the LO leakage and mirror tones appear at 100 MHz and 100.5 MHz, respectively. The corresponding synthesizer output with pre-distortion enabled, and after coefficient convergence, is given in Fig. 11. Clearly, when comparing the levels of LO leakage term without and with pre-distortion (markers M2 in Fig. 10 and Fig. 11), we can see

Table 1. Virtex-II FPGA Resource Usage

Block Name	SLICEs	MULT18	RAMB16
NCO/DDS	115		1
Pre-Distortion	79	2	
dA	54		
Control	675		
Total	**923**	**2**	**1**

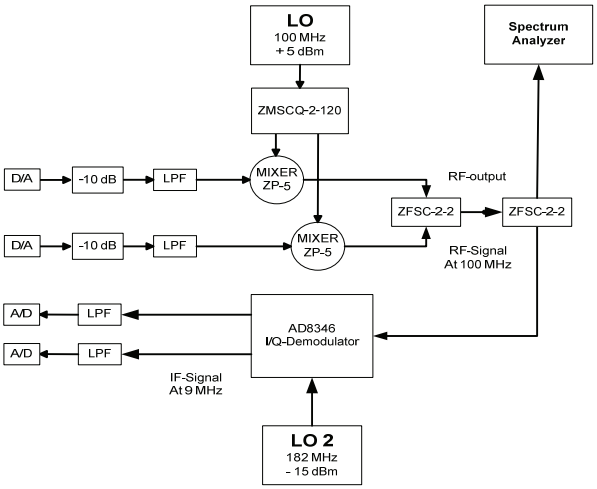

Fig. 7. Analog parts of the overall RF measurement system. I/Q-down-conversion from RF to IF is used in the feedback branch and the envelope is calculated using the I and Q components after IF sampling.

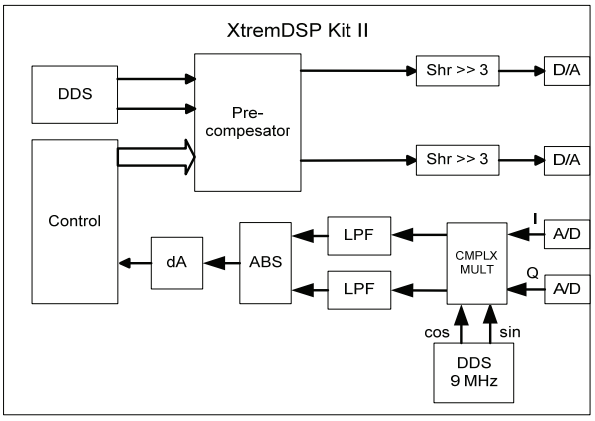

Fig. 8. Principal digital blocks of the measurement set-up.

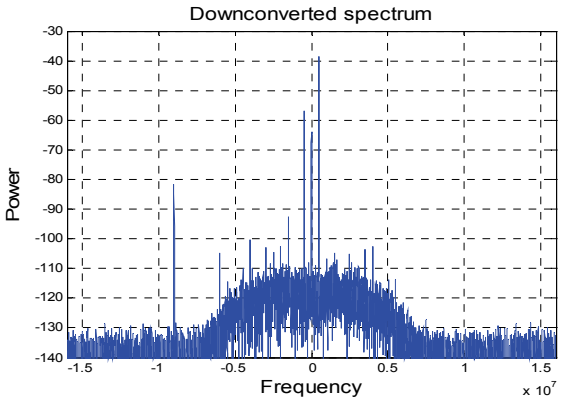

Fig. 9. Spectrum of the down-converted I/Q feedback signal.

that the pre-distortion method is able to reduce the LO leakage by 24 dB, resulting in 51 dBc overall attenuation. The mirror frequency component, in turn (markers M3), has also been further attenuated by 24 dB resulting in 53 dBc overall attenuation. Thus overall, all the spurious components are at least 50dB below the main tone, evidencing very good performance also under the actual real-time hardware implementation.

In the measurements, it was observed that the main performance limiting factor in the overall synthesizer is the feedback signal quality and dynamic range. This is easy to understand since it is exactly the feedback signal which is used, in terms of the output envelope variation, to determine the pre-distortion coefficients. This means that fairly accurate envelope detector is needed in the implementation, one way or another. On the other hand, with good-quality envelope feedback, even a very low quality I/Q modulator with strong spurious components can be efficiently pre-distorted.

5. CONCLUSIONS

This article addressed the signal processing and real-time prototype implementation of I/Q modulation based frequency synthesizer. A simple iterative digital pre-distortion method was developed, utilizing output envelope feedback, to control the unavoidable analog circuit impairments in the I/Q modulator. Also a real-time prototype implementation of the overall digital core of the synthesizer was given. By connecting the digital hardware to actual I/Q modulator, accompanied with feedback implementation, proper operation and performance of the complete synthesizer was then demonstrated and measured. Spurious-free dynamic range in the order of 50dB and beyond was demonstrated through the RF measurements.

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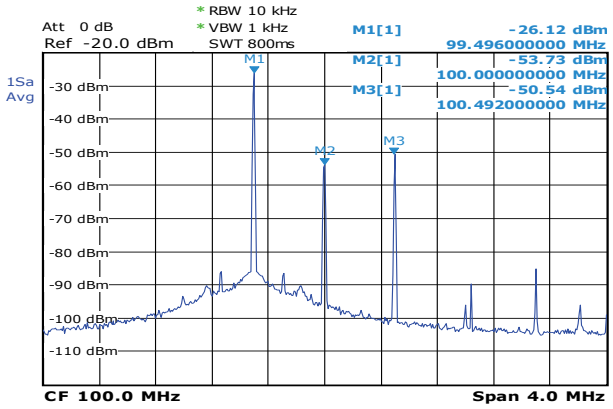

Fig. 10. Measured synthesizer output spectrum without pre-distortion.

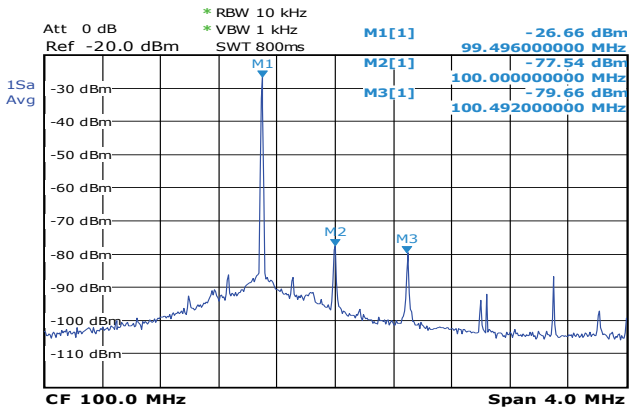

Fig. 11. Measured synthesizer output spectrum with pre-distortion enabled.