A Low-Cost Digital Self-Interference Cancellation Structure for Full-Duplex Communications

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***Abstract*—In full-duplex communications, existing digital self-interference cancellation (DSIC) scheme cancels strong self-interference (SI) in digital domain. To sample the strong self-interference, a high-performance analog-to-digital converter (AD-C) is adopted and leads to a high cost. To reduce the cost of the DSIC stage, this paper proposes a novel DSIC scheme, in which the reconstructed SI is converted to analog form and subtracted from the incoming signal before the ADC stage. Then the ADC samples only the weak user signal and doesn't require high performance. This paper analyzes the signal-to-interference-plus-noise power ratio achieved by the proposed DSIC scheme and derives the closed-form expression. In addition, comparisons show that the proposed DSIC scheme is far more cost-effective than existing DSIC scheme. At the end, various simulations verify the ability of the proposed DSIC scheme to reduce the cost.**

***Index Terms*—Full-duplex, digital self-interference cancellation, analog-to-digital converter, digital-to-analog converter, cost.**

I. Introduction

Currently, full-duplex radios adopt the analog self-interference (SI) cancellation (ASIC) scheme and the digital SI cancellation (DSIC) scheme to cancel SI [1]–[4] to avoid the significant receiver sensitivity loss and have a generalized structure as shown in Fig. 1. To eliminate the requirement for the ASIC capacity and sequentially reduce the complexity of the ASIC circuit, the DSIC stage has to provide a significant suppression of SI. For the conventional DSIC (C-DSIC) scheme shown in Fig. 1, the performance of the analog-to-digital converter (ADC) must be sufficiently high to avoid introducing too strong quantization noise. Since the high-performance ADC is always expensive, the C-DSIC scheme costs a lot of money.

To reduce the cost of the high-performance DSIC stage, this paper proposes a mixed-domain based DSIC (M-DSIC) scheme, which reconstructs SI in digital domain, then converts it to analog form, and finally subtracts it from the incoming signal before the ADC stage. Then the ADC samples only the weak user signal and thus does not require high performance, which leads to a significant reduction of the cost of the DSIC stage.

II. The Proposed M-DSIC Structure

In this section, we first briefly introduce the main idea of the proposed M-DSIC scheme, then present the system and signal models, and finally derive the signal-to-interference-plus-noise power ratio (SINR) achieved at the decoder stage.

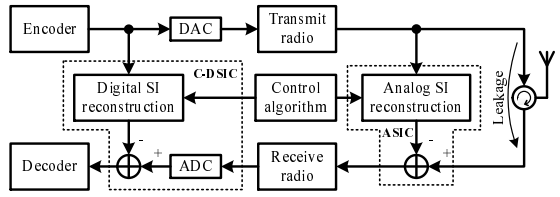

Fig. 1. Existing full-duplex radio.

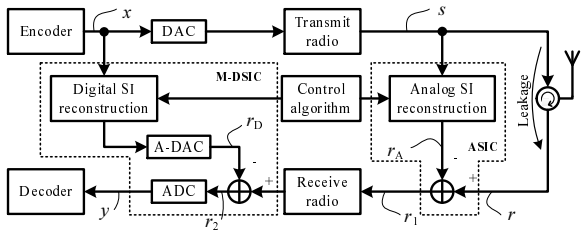

Fig. 2. Full-duplex radio configured with the M-DSIC scheme.

A. Main Idea of the Proposed M-DSIC Scheme

The proposed M-DSIC scheme is shown in Fig. 2. The information signal, generated by the encoder, is converted to analog form by the DAC and then up-converted to radio frequency by the transmit radio for channel transmission. Through the leakage path of the circulator, the transmitted signal couples into the receive chain.

In the front of the receive chain, the received signal subtracts the output of the analog SI reconstruction circuit to cancel the strong SI, targeting to avoid saturating the receive chain. Then the resulting signal is down-converted by the receive radio and fed to the M-DSIC stage, at which the down-converted signal subtracts the analog version of the output of the digital SI reconstruction module to clean out the SI left by the ASIC stage. Finally the ADC samples the desired user signal and feeds the sample points to the decoder.

B. Signal Flow

This subsection models the signals shown in Fig. 2 with their lowpass equivalent forms.

1) Transmitted Signal: The transmitted signal is the radio frequency version of the sum of the information signal x and the DAC-induced quantization noise q_1, given by

$$s = x + q_1. \tag{1}$$

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In this paper, quantization noise is considered as an additive independent noise [5].

2) ASIC: The ASIC stage subtracts the reconstructed SI generated by the analog reconstruction circuit from the received signal, which consists of the strong SI, the weak user signal r_{U}, and the receiver noise n, and yields

$$r_1 = (h_{\mathrm{SI}} - h_1) \cdot s + r_{\mathrm{U}} + n, \tag{2}$$

where h_{SI} represents the leakage path of the circulator and h_1 is the reconstruction parameter of the analog SI reconstruction circuit. After being down-converted by the receive radio, r_1 is fed to the M-DSIC stage.

3) M-DSIC: With a reconstruction parameter h_2, the digital SI reconstruction module generates an adjusted version of the information signal, which is then converted by the A-DAC to analog form, given by

$$r_{\mathrm{D}} = h_2 \cdot x + q_2, \tag{3}$$

where q_2 is the quantization noise introduced by the A-DAC. Subtracting r_{D} from r_1 yields

$$r_2 = r_1 - r_{\mathrm{D}}, \tag{4}$$

which is sampled by the ADC and fed to the decoder. The sample sequence, called the final signal, is given by

$$y = r_2 + q_3, \tag{5}$$

where q_3 is the quantization noise introduced by the ADC.

4) Final Signal: Substituting (1)$\sim$(4) into (5) yields

$$y = r_{\mathrm{U}} + (h_{\mathrm{SI}} - h_1 - h_2) \cdot x + (h_{\mathrm{SI}} - h_1) \cdot q_1 - q_2 + q_3 + n, \tag{6}$$

where $(h_{\mathrm{SI}} - h_1 - h_2)x + (h_{\mathrm{SI}} - h_1)q_1$ is the residual SI. At the ASIC stage, h_1 is tuned to approach to h_{SI} to cancel x and q_1. At the DSIC stage, h_2 is tuned to approach to $h_{\mathrm{SI}} - h_1$ to further cancel x.

C. SINR Performance

At the decoder stage, the decoding performance is determined by the SINR of y, which is defined as the power ratio of the user signal to the sum of all other components, computed as

$$\mathrm{SINR_M} = \frac{P_{\mathrm{U}}}{\frac{\|h_{\mathrm{SI}}\|^2}{G_A}\left(\frac{P_x}{G_D} + P_1\right) + P_2 + P_3 + P_{\mathrm{n}}}, \tag{7}$$

where $G_D = \|h_{\mathrm{SI}} - h_1\|^2 / \|h_{\mathrm{SI}} - h_1 - h_2\|^2$ and $G_A = \|h_{\mathrm{SI}}\|^2 / \|h_{\mathrm{SI}} - h_1\|^2$ are the capacities of the DSIC stage and the ASIC stage, respectively, P_{U}, P_x, P_1, P_2, P_3, and P_{n} are the powers of r_{U}, x, q_1, q_2, q_3, and n, respectively. Below we derive P_1, P_2, and P_3 by introducing the concept of the dynamic range to simplify (7).

1) Dynamic Range: For a commercial data converter, one of the most important specifications is the ratio of the full-scale range (FSR) to the power of the quantization noise introduced by itself, which is an unchangeable hardware parameter and measured with the unit of "effective number of bits (ENOB)". Thus the FSR must be as low as possible to reduce the power of the quantization noise. However if the FSR is lower than the peak power of the input signal, the data converter is saturated. Hence the optimal case is that the FSR is exactly equal to the peak power of the input signal and the corresponding signal-to-quantization-noise power ratio at the output port of the data converter is called the dynamic range, given in decibel form by [6]

$$10\lg(D) = 6.02 \cdot B + 4.77 - 10\lg(\Gamma), \tag{8}$$

where Γ is the peak-to-average-power ratio (PAPR) of the input signal and B is the ENOB of the data converter provided by manufacturer (If the specification of "signal-to-noise-and-distortion ratio", denoted by γ (dB), is provided, the corresponding ENOB can be computed with $B = (\gamma - 1.76)/6.02$ [6]). In this paper, we consider that the FSRs of the DAC, the A-DAC, and the ADC have already been tuned and are equal to the peak powers of the input signals, respectively.

2) Derivations of P_1, P_2, and P_3: With the concept of dynamic range, P_1 and P_2 are computed as

$$P_1 = \frac{P_x}{D_1} \text{ and } P_2 = \frac{\mathrm{E}[\|h_2 \cdot x\|^2]}{D_2} = \frac{\|h_2\|^2 P_x}{D_2}, \tag{9}$$

respectively, where D_1 and D_2 are the dynamic ranges of the DAC and the A-DAC, respectively, $\mathrm{E}[\cdot]$ represents the mean value of a variable, and $\|\cdot\|$ represents the modulus of a complex number. Substituting (1)$\sim$(3) into (4) yields $r_2 = r_{\mathrm{U}} + (h_{\mathrm{SI}} - h_1 - h_2) \cdot x + (h_{\mathrm{SI}} - h_1) \cdot q_1 - q_2 + n$ and P_3 is computed with the concept of dynamic range as

$$P_3 = \frac{E[\|r_2\|^2]}{D_3} = \frac{P_{\mathrm{U}} + \frac{\|h_{\mathrm{SI}}\|^2}{G_A}\left(\frac{P_x}{G_D} + P_1\right) + P_2 + P_{\mathrm{n}}}{D_3}, \tag{10}$$

where D_3 is the dynamic range of the ADC.

3) Achieved SINR: Substituting (9) and (10) into (7) yields (11), where $\|h_2\|/\|h_{\mathrm{SI}} - h_1\|$ varies in the range $\left[1 - 1/\sqrt{G_D},\ 1 + 1/\sqrt{G_D}\right]$ due to the inaccuracy of the digital SI reconstruction module and $\|h_{\mathrm{SI}}\|^2$ is the SI reduction provided by the circulator. Intuitively, $\mathrm{SINR_M}$ is dependent on the dynamic ranges of the DAC, the A-DAC, and the ADC in addition to the capacities of the ASIC and DSIC stages.

III. Performance Analysis

This section answers whether the M-DSIC scheme is cost-effective or not. We first discuss how to build the M-DSIC structure and then detail how much cost the M-DSIC structure saves relative to the C-DSIC structure.

A. How to Build the M-DSIC Structure?

This subsection provides a guide for design engineers to build the M-DSIC structure. If the A-DAC and the ADC are ideal, i.e., $D_2 = \infty$ and $D_3 = \infty$, $\mathrm{SINR_M}$ in (11) reaches

$$\text{SINR}_\text{M} = \frac{P_\text{U}}{\frac{P_\text{U}}{D_3} + \frac{\|h_\text{SI}\|^2}{G_A}\left(\frac{1}{G_D}+\frac{1}{D_1}+\frac{1}{D_2}\frac{\|h_2\|^2}{\|h_\text{SI}-h_1\|^2}\right)(1+\frac{1}{D_3})P_x + (1+\frac{1}{D_3})P_\text{n}}. \tag{11}$$

to the maximum value $\frac{P_\text{U}}{\|h_\text{SI}\|^2/G_A(1/G_D+1/D_1)P_x+P_\text{n}}$. However, D_2 and D_3 are always finite in practice and SINR_M is degraded. Therefore this subsection makes trade-offs between SINR_M and D_2, D_3, respectively.

1) Requirement for the A-DAC: As D_2 decreases from ∞ to $\frac{\|h_2\|^2}{\|h_\text{SI}-h_1\|^2(1/G_D+1/D_1)}$, SINR_M in (11) is degraded from $\frac{P_\text{U}}{P_\text{U}/D_3+\|h_\text{SI}\|^2/G_A(1/G_D+1/D_1)(1+1/D_3)P_x+(1+1/D_3)P_\text{n}}$ down to $\frac{P_\text{U}}{P_\text{U}/D_3+2\|h_\text{SI}\|^2/G_A(1/G_D+1/D_1)(1+1/D_3)P_x+(1+1/D_3)P_\text{n}}$, by no more than 3 dB. Thus we consider SINR_M approximately does not change if $D_2 \in \left[\frac{\|h_2\|^2}{\|h_\text{SI}-h_1\|^2(1/G_D+1/D_1)},\ \infty\right)$. Substituting the maximum value of $\|h_2\|/\|h_\text{SI}-h_1\|$ given behind (11), this limitation for D_2 is derived as

$$D_2 \in \left[\frac{\left(1+1/\sqrt{G_D}\right)^2}{1/G_D+1/D_1},\ \infty\right), \tag{12}$$

which provides a guide for the design of the A-DAC. Naturally, a question is raised: Does there exist a commercial product whose dynamic range satisfies (12)? This question will be answered below.

We can derive $\left(\sqrt{D_1}+1\right)^2 - \frac{\left(1+1/\sqrt{G_D}\right)^2}{1/G_D+1/D_1} = \frac{\left(\sqrt{G_D}\left(2\sqrt{D_1}+1\right)-D_1\right)^2+2D_1^{1.5}\left(\sqrt{D_1}+1\right)^2}{(G_D+D_1)\left(2\sqrt{D_1}+1\right)} \geq 0$ for arbitrary G_D and D_1 and thus $D_2 = \left(\sqrt{D_1}+1\right)^2$ always satisfies (12). Considering that existing communication standards [7] require the transmit chain to transmit signals with an error vector magnitude of far smaller than 1, the DAC's dynamic range must satisfy $\sqrt{D_1} \gg 1$. Then $D_2 = \left(\sqrt{D_1}+1\right)^2 \approx D_1$ satisfies (12), i.e., using the same series of product as the DAC as the A-DAC can avoid significant degradation of SINR_M. Hence the commercial product whose dynamic range satisfies (12) always exists.

2) Requirement for the ADC: As D_3 decreases from ∞ to $1+\frac{P_\text{U}}{\|h_\text{SI}\|^2/G_A\left(1/G_D+1/D_1+1/D_2\|h_2\|^2/\|h_\text{SI}-h_1\|^2\right)P_x+P_\text{n}}$, SINR_M in (11) is degraded from $\frac{P_\text{U}}{\|h_\text{SI}\|^2/G_A\left(1/G_D+1/D_1+1/D_2\|h_2\|^2/\|h_\text{SI}-h_1\|^2\right)P_x+P_\text{n}}$ down to $\frac{P_\text{U}}{2\|h_\text{SI}\|^2/G_A\left(1/G_D+1/D_1+1/D_2\|h_2\|^2/\|h_\text{SI}-h_1\|^2\right)P_x+2P_\text{n}}$, by only 3 dB. In other words, SINR_M almost does not change if $D_3 \geq 1+\frac{P_\text{U}}{\|h_\text{SI}\|^2/G_A\left(1/G_D+1/D_1+1/D_2\|h_2\|^2/\|h_\text{SI}-h_1\|^2\right)P_x+P_\text{n}}$. Substituting (12) into this limitation for D_3 yields the improved requirement for the ADC, given by

$$D_3 \in \left[1+\frac{P_\text{U}}{\frac{\|h_\text{SI}\|^2}{G_A}\left(\frac{1}{G_D}+\frac{1}{D_1}\right)P_x+P_\text{n}},\ \infty\right), \tag{13}$$

which provides a guide for the design of the ADC. Does there exist a commercial product whose dynamic satisfies (13)? This question will be answered below.

It is clear that $D_3 = P_\text{U}/P_\text{n}+1$ always satisfies (13) for arbitrary G_D and D_1. (1) In most case, the user signal is weak and $D_3 = P_\text{U}/P_\text{n}+1$ is a rather low requirement for commercial products. For example, in the LTE communication standard [7], detecting a 64-ray quadrature amplitude modulation signal requires a signal-to-noise ratio of 19.7 dB, i.e., $D_3 = P_\text{U}/P_\text{n}+1 = 10^{19.7/10}+1 = 93.33$, corresponding to only 4.15-bit ENOB even the signal has a PAPR of 10 dB. Lots of commercial products which have more than 4.15-bit ENOB can be found, such as the AD9286 [8] which has 7.9-bit ENOB. (2) An opposite case is that the incoming user signal is too strong and no existing commercial product can provide a dynamic range as high as $P_\text{U}/P_\text{n}+1 \approx P_\text{U}/P_\text{n}$. It's an exceptionally rare case in existing application scenarios since not only the proposed M-DSIC but also the C-DSIC and the well-developed half-duplex receiver can not handle this strong incoming user signal without causing sensitivity loss.

3) Receiver Sensitivity Loss: Substituting (12) and (13) into (11) yields the variation range of SINR_M, given by

$$\text{SINR}_\text{M} \in \left[\frac{P_\text{U}}{\left(2+\frac{P_\text{SI}}{P_\text{U}+P_\text{rSI}+P_\text{n}}\right)(P_\text{rSI}+P_\text{n})+P_\text{rSI}},\ \frac{P_\text{U}}{P_\text{rSI}+P_\text{n}}\right), \tag{14}$$

where $P_\text{rSI} = \frac{\|h_\text{SI}\|^2}{G_A}\left(\frac{1}{G_D}+\frac{1}{D_1}\right)P_x$ is the power of the residual SI. The ratio of SINR_M's upper bound to its lower bound is the maximum potential receiver sensitivity loss caused by the tradeoff in (12) and (13), i.e.,

$$\text{SINR}_\text{Loss} \leq 2+\frac{P_\text{rSI}}{P_\text{U}+P_\text{rSI}+P_\text{n}}+\frac{P_\text{rSI}}{P_\text{rSI}+P_\text{n}}, \tag{15}$$

which is discussed as follows. (1) With ideal ASIC and M-DSIC stages, the SI is cleaned out, i.e., $P_\text{rSI}=0$, and then $\text{SINR}_\text{Loss} \leq 2$. (2) With well-designed ASIC and M-DSIC stages, the power of the residual SI is reduced down to the level of the receiver noise [1], i.e., $P_\text{rSI}=P_\text{n}$, and then $\text{SINR}_\text{Loss} \leq 5/2+1/\left(P_\text{U}/P_\text{n}+2\right) < 3$. (3) With low-performance ASIC and M-DSIC stages, the residual SI is far stronger than the receiver noise, i.e., $P_\text{rSI} \gg P_\text{n}$, and then $\text{SINR}_\text{Loss} \leq 3+1/\left(P_\text{U}/P_\text{rSI}+1\right) < 4$. The former discussions show that the receiver sensitivity loss caused by the tradeoff in (12) and (13) is always smaller than 6 dB for arbitrary G_A and G_D.

To summarize, (12) and (13) balance the realizability and the SINR performance for the M-DSIC scheme well.

B. Is the M-DSIC Structure Cost-Effective?

In this subsection, comparisons between the M-DSIC scheme and the C-DSIC scheme are performed in terms of cost. We first derive the expression of the SINR achieved by the "C-DSIC+ASIC" structure, then detail a typical application scenario, and finally comparisons are performed.

TABLE I
COMPARISONS BETWEEN THE M-DSIC SCHEME AND THE C-DSIC SCHEME

C-DSIC				M-DSIC[1]							Advantages	
ADC			SINR_C (dB)	A-DAC			ADC			SINR_M (dB)	Cost saving	$\frac{\text{SINR}_\text{M}}{\text{SINR}_\text{C}}$ (dB)
Product name	ENOB (bits)	Price[2] (US$)		Product name	ENOB (bits)	Price[2] (US$)	Product name	ENOB (bits)	Price[2] (US$)			
ISLA214S50 [9]	11.8	185/1	-0.87	DAC3174 [10]	12.3	18.9/2	AD9286 [8]	7.9	36/2	-0.06	81.3%	0.81
ADS54J66 [11]	11.4	596.5/4	-1.85								76.8%	1.79
ADS54J54 [12]	10.9	495/4	-3.53								72.0%	3.47
ADS5407 [13]	10.3	239.95/2	-6.17								71.2%	6.11
ADS5404 [14]	9.8	218.75/2	-8.73								68.4%	8.67

[1] To build the addition circuit, the M-DSIC adopts a piece of ADP-2-1 [15], which costs 7.15 dollars and is not listed in the table due to space limitation.
[2] Commercial products may integrate two or more entities into one single package. To be fair, the entity price, computed with $\frac{\text{Package price}}{\text{Number of entities}}$, is considered.

1) SINR Performance of the "C-DSIC+ASIC" Structure: The achievable SINR performance of the "C-DSIC+ASIC" structure, denoted by SINR_C, can be derived by following the same derivation steps as in subsections II-B and II-C. Due to the space limitation, we directly give the expression as

$$\text{SINR}_\text{C} = \frac{P_\text{U}}{\frac{P_\text{U}}{D_3^{'}} + \frac{\|h_\text{SI}\|^2}{G_A}\left(\frac{1}{G_D}+\frac{1}{D_1}+\frac{1}{D_3^{'}}+\frac{1}{D_1 D_3^{'}}\right)P_x + (1+\frac{1}{D_3^{'}})P_\text{n}}, \tag{16}$$

where $D_3^{'}$ is the dynamic range of the ADC adopted in the C-DSIC structure.

2) Typical Application Scenario: Take the LTE home base station [7] for example. The LTE home base station transmits a 100 MHz bandwidth signal with a PAPR of 10 dB at a transmit power of 20 dBm and receives a user signal of -90 dBm at a noise power spectral density of -174 dBm. In the transmit chain, a piece of DAC3174 [10] is used as the DAC and the circulator provides a SI reduction of 15 dB. The capacities of the ASIC stage and the DSIC stage are 33 dB and 69 dB, respectively. Besides, the DAC, the A-DAC, and the ADC operate with a sample rate of 500 Msps.

3) Comparisons: In Table I, comparisons between the C-DSIC scheme and the M-DSIC scheme are performed to answer whether the M-DSIC scheme is cost-effective. The M-DSIC structure and the C-DSIC structure are built carefully with commercial products to achieve the resemblant SINR performances and then the advantages of the M-DSIC scheme over the C-DSIC scheme are listed in terms of cost saving and SINR improvement.

Adopting a piece of DAC3174 [10], a piece of AD9286 [8], and a piece of ADP-2-1 [15] as the A-DAC, the ADC, and the addition circuit, respectively, the M-DSIC structure costs 34.6 dollars and achieves $\text{SINR}_\text{M} = -0.06$ dB (Here, SINR_M is computed with (11), where the item $\|h_2\|/\|h_\text{SI} - h_1\| \approx 1$ since $G_D = 69$ dB $\gg 1$). With different series of commercial ADCs, the C-DSIC structure costs different money and achieves different SINRs, seeing Table I. For instance, using a piece of ISLA214S50 to build the C-DSIC structure costs 185 dollars and achieves $\text{SINR}_\text{C} = -0.87$ dB. Visually, the M-DSIC scheme provides higher SINR at the cost of much less money than the C-DSIC scheme and thus is rather cost-effective.

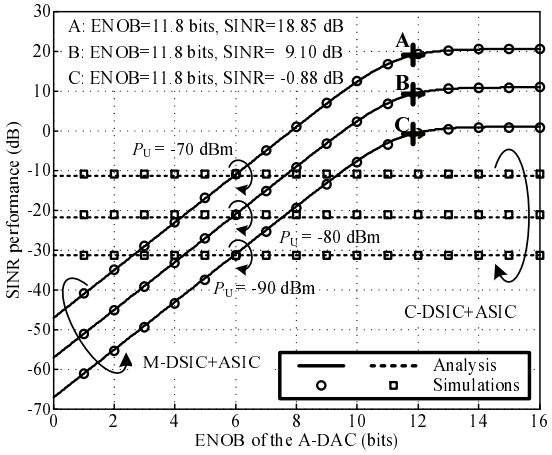

Fig. 3. SINR performance vs. ENOB of the A-DAC in case of different user signal strengths.

IV. SIMULATIONS

In this section, various simulations are performed with Matlab (developed by the MathWorks Inc.) to verify the proposed M-DSIC scheme. The configuration parameters described in subsubsection III-B2 are adopted in the simulations. Besides, the radio frequency and the intermediate frequency are 2350 MHz and 120 MHz, respectively. For comparisons, we also simulate the "C-DSIC+ASIC" structure (Seeing Fig. 1) where the C-DSIC structure adopts the same ADC as the one employed by the M-DSIC structure.

A. Impact of the A-DAC on the SINR Performance

The impact of the A-DAC on the SINR performance is simulated and plotted in Fig. 3, where the ADC is configured with 6-bit ENOB. The horizontal coordinates of "A", "B", and "C" are computed with (12). When the ENOB of the A-DAC varies from 16 bits to 11.8 bits, the SINR achieved by the "M-DSIC+ASIC" structure approximately doesn't decrease. In contrast, significant SINR degradation is caused when the

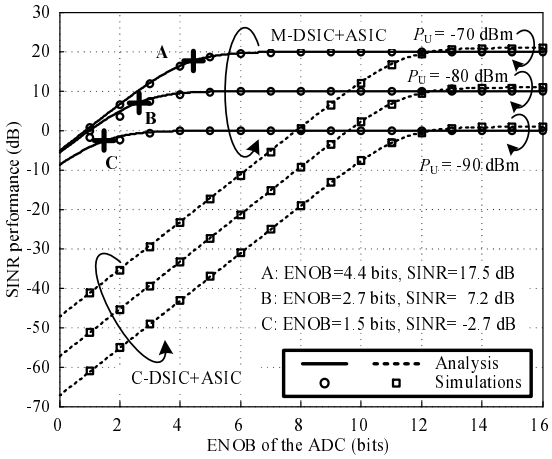

Fig. 4. SINR performance vs. ENOB of the ADC in case of different user signal strengths.

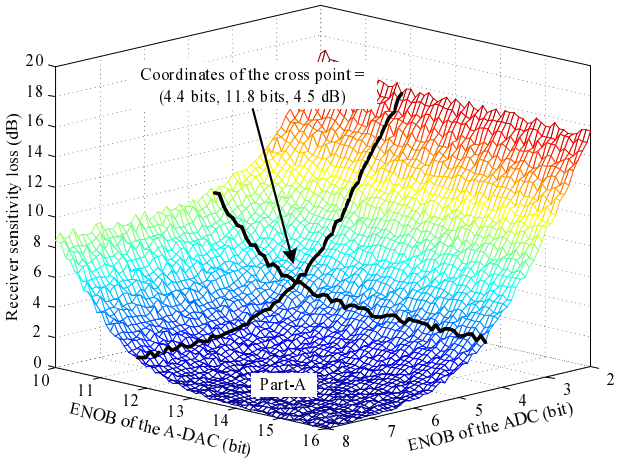

Fig. 5. Receiver sensitivity loss $\mathrm{SINR}_{\mathrm{Loss}}$ vs. ENOBs of the ADC and the A-DAC in case of $P_{\mathrm{U}} = -70$ dBm.

ENOB of the A-DAC is smaller than 11.8 bits. Thus (12) is verified to be a good tradeoff. Besides, the analysis and simulation results show that the "M-DSIC+ASIC" structure achieves higher SINR than the "C-DSIC+ASIC" structure by increasing the ENOB of the A-DAC.

B. Impact of the ADC on the SINR Performance

The impact of the ADC on the SINR performance is simulated and plotted in Fig. 4, where the A-DAC is configured with 12.3-bit ENOB. The points "A", "B", and "C" are called the turning points and their horizontal coordinates are computed with (13). For the "M-DSIC+ASIC" structure, the analysis and simulation results show significant SINR degradation at left of these turning points but almost don't change at right of these turning points. Thus (13) is verified to be a good tradeoff. For the "C-DSIC+ASIC" structure, the analysis and simulation results show significant SINR degradation if the ENOB of the ADC is smaller than 12-bit. This phenomenon verifies the ability of the M-DSIC scheme to eliminate the requirement for the ADC.

C. Receiver Sensitivity Loss

The tradeoff in (12) and (13) leads to the receiver sensitivity loss, which is simulated and plotted in Fig. 5. In Part-A, the dynamic ranges of the A-DAC and the ADC satisfy (12) and (13), respectively and the maximum receiver sensitivity loss in part-A is equal to 4.5 dB, which fits the discussions about the upper bound of the receiver sensitivity loss in subsection III-A3.

V. Conclusion

In existing full-duplex communications, high-performance DSIC stage requires high-performance ADC, which is expensive or even not off-the-shelf. Hence eliminating the requirement for the ADC's performance has significant engineering value. For this purpose, this paper proposes the M-DSIC scheme, which is verified to be able to eliminate the requirement for the ADC's performance significantly by analyses and simulations. Moreover, evaluations based on commercial products are performed and show that the M-DSIC scheme is far more cost-effective than the C-DSIC scheme.

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