

# Performance of a MC-CDMA Baseband Demonstrator for Beyond 3G systems

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## ABSTRACT

**The MC-CDMA transmission technique is seen as a candidate for beyond 3G systems. It benefits from the high bandwidth efficiency of multi-carrier systems and the flexibility and granularity offered by CDMA for the allocation of resources.**

**In the framework of the IST MATRICE European Project, a MC-CDMA baseband hardware demonstrator has been developed. This paper describes its specifications, details its complexity and presents the measured performances.**

## I. INTRODUCTION

The third generation terrestrial mobile system (UMTS-UTRA) is currently being launched. It aims at offering a large variety of services (circuit and packet services, low to high bit rates), as well as greater capacity compared to second-generation systems (e.g. GSM). The evolution from 2G to 3G represents a change in many aspects: new technology, change of focus from voice to mobile multimedia, simultaneous support of several QoS classes in a single radio interface. Despite the high capacity offered by the 3G technology, the rapid growth of Internet services and increasing interest in portable computing devices are likely to create a strong demand for high-speed wireless data services, presumably with a maximum information bit rate of more than 2-20 Mbps in a vehicular environment and possibly 50-100 Mbps in indoor to pedestrian environments, using a 50-100 MHz bandwidth [1]. Specially in the downlink, high throughput will be needed, since the number of downloads of large data files from web sites and servers will increase, and broadcast/multicast services may become a reality.

It is clear that provision of such high bit rates requires the development of a new technology. One of the most promising candidate techniques for achieving high data rate transmission in a mobile environment is multi-carrier CDMA (MC-CDMA) which divides a wide signal bandwidth into several sub-channels, where several information bearing signals can coexist by using code separation. Research at several universities and R&D laboratories has already pointed out MC-CDMA as a

potential technique for the broadband component of future cellular systems [2]. However to provide a comprehensive picture for the standardisation of future broadband mobile systems, considerable work is still required, particularly when it concerns the integration of several processing techniques (multiple access, coding, equalization, resource allocation, ...).

In the framework of the IST MATRICE European Project [3], a baseband hardware demonstrator has been developed to evaluate the performance of the MC-CDMA technique. This paper describes the specifications of this prototype and its performance.

The hardware demonstrator is implemented on a commercial platform which has the capability to host DSP, FPGA and I/O modules [4]. All the processing blocks have been implemented on FPGAs.

The paper is organized as follows: in section II, the demonstrator specifications are described, in section III, the mapping of functions on the used FPGAs is presented, as well as the complexity of the most critical modules, and in section IV the measured performance is given and interpreted.

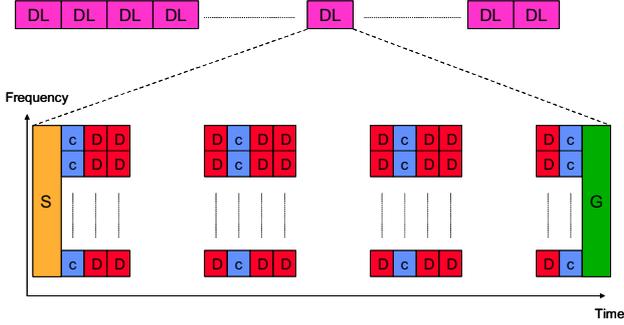
## II. SYSTEM DESCRIPTION

The main features of the radio frame of the demonstrator are the following [5]:

- Time Division Duplex mode: we consider a 28.8 ms frame of 15 slots, where the first slot of each frame is dedicated to DL transmission.
- System bandwidth equal to 20 MHz.
- FFT size:  $N = 1024$  (736 useful subcarriers and 288 null subcarriers for spectral shaping), cyclic prefix of 216 samples.
- Spreading factor: 32.
- Number of data symbols per OFDM symbol:  $736/32 = 23$ .
- Supported constellations: QPSK and 16-QAM.
- Channel coding: convolutional code with 1/2 and 3/4 coding rate (RCPC code from IEEE 802.11a standard).

The slot structure is depicted in Figure 1. It contains a synchronization sequence (S), 4 full OFDM symbols for

channel estimation (C), 24 OFDM symbols with data (D) and a guard interval (G).



**Figure 1 : Frame structure.**

The synchronization sequence is made of the 256 chips primary sequence used in UMTS [6]. The transmission between Tx and Rx is performed at an Intermediate Frequency (IF) which is generated digitally.

Table 1 presents the service classes that have been defined according to the combination of some modulation and coding schemes. Table 2 gives bit rates that can be achieved with each class depending on the number of allocated spreading codes. The demonstrator can support bit rates from 288 Kbps up to 27.6 Mbps, with a very good granularity.

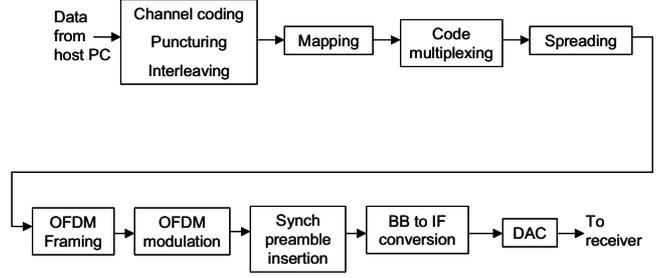
	$R_C$	Modulation
Class 1	1/2	QPSK
Class 2	3/4	QPSK
Class 3	1/2	16-QAM
Class 4	3/4	16-QAM

**Table 1 : Service classes.**

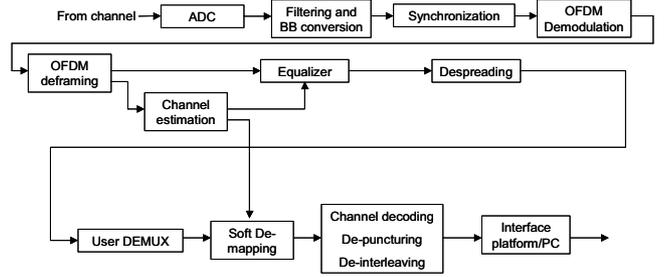
Data rate (Mbits/s)	1 code	16 codes	32 codes
Class 1	0.288	4.6	9.2
Class 2	0.431	6.9	13.8
Class 3	0.575	9.2	18.4
Class 4	0.862	13.8	27.6

**Table 2 : Class bit rates.**

Figure 2 gives a functional view of the transmitter and Figure 3 presents the receiver structure. The data corresponding to an entire slot are encoded and punctured. The goal of channel bit interleaving is to avoid long sequences of consecutive corrupted bits due to channel degradations. Thanks to its particular structure, the OFDM modulation allows both frequency and time interleaving. Frequency interleaving is used to ensure that the attenuation of adjacent sub-carriers does not affect adjacent coded bits. By duality, time interleaving is designed to deal with deep fades of the received signal strength over several consecutive OFDM symbols. Only frequency interleaving is implemented in this demonstrator.



**Figure 2 : Transmitter.**



**Figure 3 : Receiver.**

Channel estimation is performed as follows [5]:

- For each received full pilot OFDM symbol, remove the known pilot modulation and perform a frequency averaging over the 2 adjacent subcarriers on each side.
- Perform a linear interpolation between 2 consecutive pilot symbols in order to get the channel estimates for the OFDM symbols transmitted in between.

The equalizer is a normalized Minimum Mean Square Error (MMSE) which applies a one tap coefficient per sub-carrier :

$$g_i[kS_F + l] = \frac{\hat{h}_i^*[kS_F + l]}{|\hat{h}_i[kS_F + l]|^2 + \lambda} \frac{1}{NORM_i[k]}; l=0, \dots, S_F - 1; k=0, \dots, 23$$

$$NORM_i[k] = \sum_{l=1}^{S_F} \frac{|\hat{h}_i[kS_F + l]|^2}{|\hat{h}_i[kS_F + l]|^2 + \lambda}$$

where  $\hat{h}_i[kS_F + l]$  is the channel estimate of the  $(kS_F + l)^{th}$  subcarrier, and  $\lambda$  is the average SNR per subcarrier. This parameter is fixed in the demonstrator ( $\lambda = 0.78$  for classes 1 and 3, and  $\lambda = 0.16$  for classes 2 and 4).

The Log Likelihood Ratios (LLR) used by the soft-demapping to improve the decoder performance are computed according to the following formula:

$$LLR_i[k] = \frac{NORM_i[k]}{S_F} \sum_{l=1}^{S_F} |\hat{h}_i[kS_F + l]|^2$$

This LLR does not correspond to the optimum LLR formulation, or even the simplified formula proposed by Kaiser [7]. On the other hand, it induces only a 0.5 dB loss for a great improvement in complexity.

The decoder is a soft-input hard-output Viterbi decoder.

### III. HARDWARE MAPPING AND COMPLEXITY

Figure 4 shows the structure of the hardware modules which are used to build the transmitter. Most of the processing blocks are integrated in a Virtex II 3 Million gates FPGA from Xilinx. The overall logic utilization is about 38%. The BB (baseband) to IF conversion module is integrated on a 1 million gates FPGA on the I/O module. *It uses 33 % of the available logic.* The samples are then converted to the analog domain with a 14-bit DAC. The transmitter and the receiver are connected by a cable. Hence the channel contains no multipath. The complexity of the main modules of the transmitter is detailed in Table 3. As expected, the OFDM module is the most resource consuming.

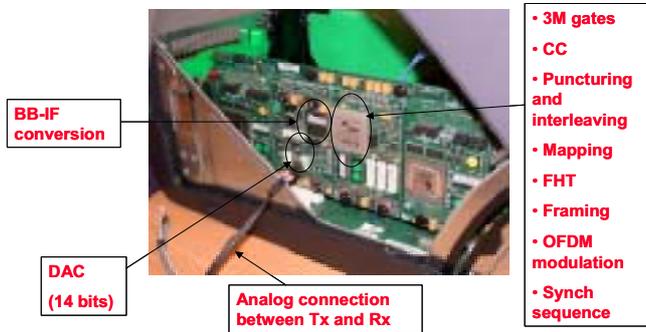


Figure 4 : Transmitter HW structure.

	Channel coding, Puncturing and Interleaving	User mux, Spreading and Framing	OFDM modulation (IFFT and CP insertion)
Slices	1200	1100	3200
Block RAMs	5	22	21
Multipliers 18x18	0	2	9

Table 3 : Transmitter complexity.

The receiver structure is depicted in Figure 5. The received IF signal is first sampled at 40MHz with a 12-bit ADC. Then the digital samples are transposed into BB and a synchronization unit detect the transmitted sequence at the beginning of each slot. These 2 operations are integrated in a 1 Million gates FPGA (logic utilization of 46 %). Once synchronization is achieved, the samples corresponding to an entire slot are stored and transferred to a 6 million gates FPGA, which performs all the remaining processing operations. The logic utilization is about 38%. The complexity of the main modules is detailed in Table 4. The channel estimation module requires a large number of block RAMs since it computes the equalizer coefficients for the entire slot. The channel decoding unit (deinterleaving, depuncturing and Viterbi decoding) uses the largest number of slices.



Figure 5 : Receiver HW structure.

	OFDM demodulation	Deframing, Channel estimation	Equalization, Despreading and User demultiplexing	Channel decoding
Slices	2500	4300	700	5500
Block RAMs	19	30	0	9
Multipliers 18x18	9	15	2	0

Table 4 : Detailed receiver complexity.

### IV. DEMONSTRATOR PERFORMANCE

In addition to the modules already described in the previous sections, the receiver includes another module to add white Gaussian noise. The performance of the demonstrator is measured by the Bit Error Rate (BER) as a function of the input Signal to Noise Ratio (SNR). The BER is measured at the output of the Viterbi decoder. The demonstrator has been validated and its performance measured with 3 different configurations:

- *Configuration 1:* full digital transmission without A/D converters or digital BB to IF and IF to BB modules. Moreover, the transmitter and receiver are perfectly synchronized.
- *Configuration 2:* analogue transmission and real synchronization but with the same sampling clock for the transmitter and the receiver.
- *Configuration 3:* analogue transmission and real synchronization with different sampling clocks for the transmitter and the receiver. Each oscillator stability is lower than 30 ppm.

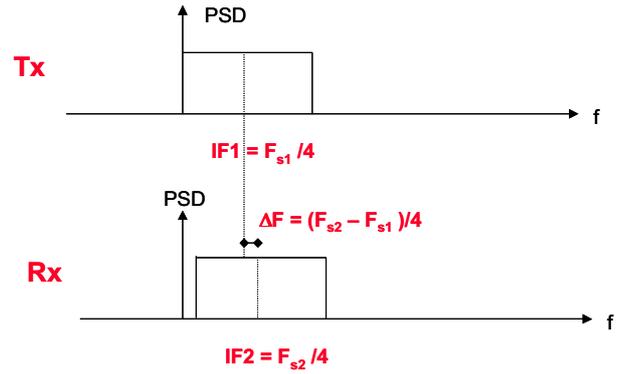
Results obtained with configuration 1 gave reference performance measurements taking into account the degradation introduced by channel estimation and fixed point processing. With the results from configuration 2, we evaluated the degradation introduced by the D/A and A/D converters as well as the BB/IF and IF/BB operations. Eventually, configuration 3 gave the final results, including the sensitivity of the receiver to sampling clock frequency offset.

Figure 6 and Figure 7 present the performances measured for classes 1 and 4 (half load, 16 codes), with the 3 configurations. The results obtained with classes 2 and 3 and also with a fully loaded system are similar.

We observe that performances obtained with configurations 1 and 2 are almost identical. This means that neither the synchronization process nor the BB to IF and IF to BB modules degrade the performance of the demonstrator.

When considering configuration 3, we observe degradation compared to 1 and 2. This cannot be explained by the direct effect of a sampling clock frequency offset. Since the precision of each oscillator is 30 ppm, the maximum value of  $\Delta T/T$  is 60 ppm and  $N\Delta T/T = 0.061$ . According to [8], this figure corresponds to a negligible degradation of the SNR.

In fact this is due to the BB to IF conversion which is done in the digital domain (Figure 8). At the transmitter, the signal is multiplied by  $e^{j2\pi nF_s T_s/4}$  to shift the spectrum by  $F_s/4$ . The receiver performs the dual operation with a different sampling clock. Hence, this produces a carrier frequency offset  $\Delta F T = (1/4T_{S1} - 1/4T_{S2}) T_{S2} \approx \Delta T/4T$ .



**Figure 8 : Carrier frequency offset.**

The carrier frequency offset has 2 effects:

- Introduction of Inter Carrier Interference (ICI) at the output of the FFT. This can be modelled by an additional Gaussian noise.
- Attenuation and rotation of each subcarrier.

The degradation caused by a carrier frequency offset  $\Delta F$  has been evaluated by Steendam and Moeneclay [8]:

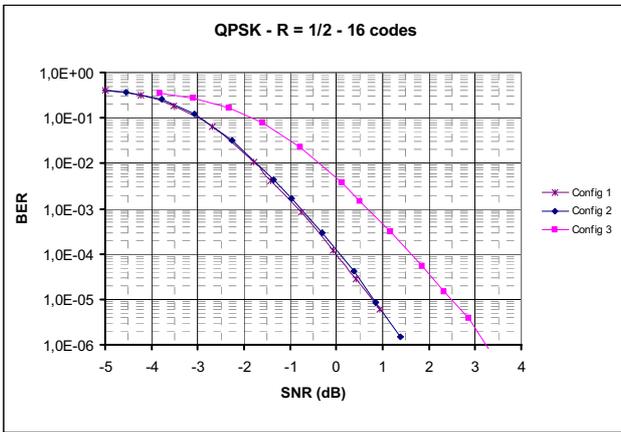
$$D_q \approx -10 \log \left( \left| \frac{\sin(\pi N \Delta F T_s)}{N \sin(\pi \Delta F T_s)} \right|^2 \right) + 10 \log \left( 1 + \frac{P}{\sigma^2} \left( 1 - \left| \frac{\sin(\pi N \Delta F T_s)}{N \sin(\pi \Delta F T_s)} \right|^2 \right) \right)$$

To obtain this expression, the authors assumed that the equalizer was able to perfectly compensate for the attenuation and phase rotation introduced by the carrier frequency offset on each sub-carrier.  $P$  is the power allocated to each code, and  $\sigma^2$  is the noise variance.

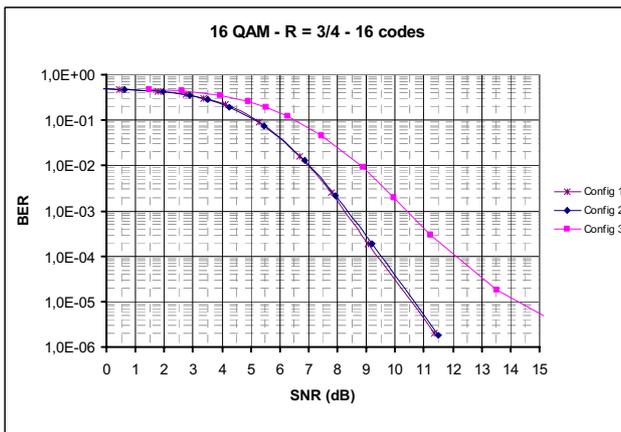
Figure 9 presents the BER measurements made with a floating point simulation chain implementing the same algorithms. The simulations have been performed with a variable carrier frequency offset, for class 4 with a full load. For  $N\Delta F T < 0.01$ , the degradation is negligible as predicted by the model of Steendam and Moeneclay. On the other hand, the degradation observed for  $N\Delta F T = 0.02$  and  $0.03$  is much more severe than the one predicted by the model. This is due to the channel estimation process which is also corrupted by the carrier frequency offset. For high level of interference, the channel estimation is inaccurate and the equalizer is not able to perfectly compensate for the phase rotation introduced by the carrier frequency offset on each sub-carrier.

With the demonstrator, we have  $N = 1024$  and  $\max(\Delta F T) = 15 \cdot 10^{-6}$ , thus  $\max(N\Delta F T) \approx 0.015$ . Hence the loss observed when the transmitter and receiver have different sampling clocks is explained by the carrier frequency offset induced by the BB-IF and IF-BB processes.

Figure 10 and Figure 11 compare the performance of the 4 classes for configurations 2 and 3. We observe that, due to the degradation introduced by the carrier frequency offset, the gap between classes 2 and 3 is reduced to 1 dB at a BER of  $10^{-5}$ . This means that class 2 is almost useless with configuration 3. The introduction of RF impairments can annihilate the interest for a given modulation and coding scheme.



**Figure 6 : Performance of Class 1 (half load).**



**Figure 7 : Performance of Class 4 (half load).**

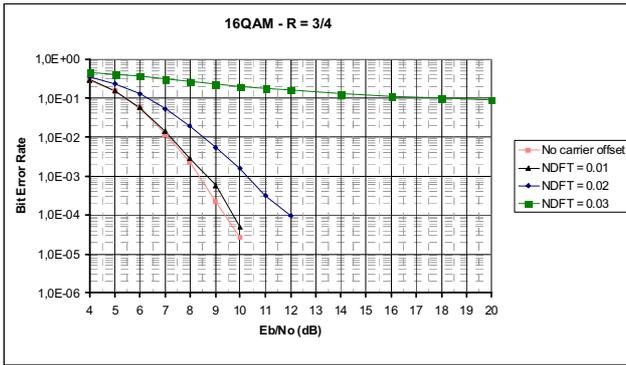


Figure 9 : BER degradation due to carrier frequency offset (full load).

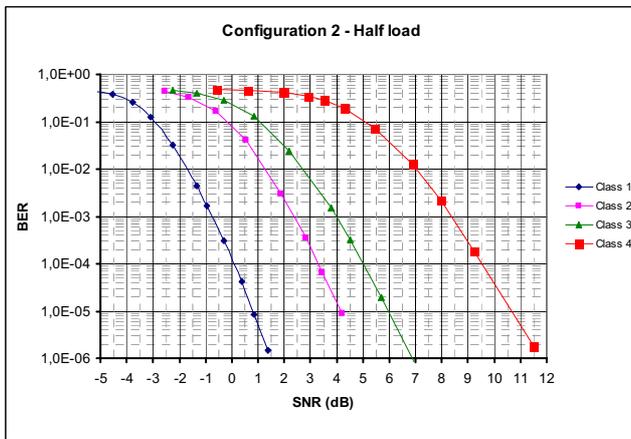


Figure 10 : Class comparison for configuration 2.

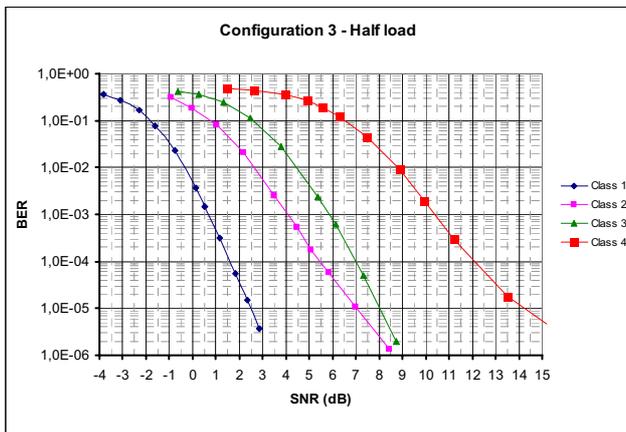


Figure 11 : Class comparison for configuration 3.

## V. CONCLUSION

In this paper, we have described a MC-CDMA baseband hardware demonstrator that has been developed for a beyond 3G system. The mapping of the functions on the used FPGAs has been presented, as well as the evaluated complexity for the main processing blocks. We have then

measured the performance of the demonstrator and its sensitivity to sampling clock and carrier frequency offsets. We observed degradation when transmitter and receiver have asynchronous sampling clocks. This is mainly explained by the carrier frequency offset created by the BB to IF conversion, even if it is implemented digitally. This demonstrator is the first step towards a complete MIMO MC-CDMA prototype, including an RF unit, that is been developed in the IST 4MORE European Project [9].

## ACKNOWLEDGEMENTS

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