

BER Optimization for Micro Power Receivers Using Quick and Accurate System Simulation

Thomas Stücker*, Niels Christoffers†, Rainer Kokozinski† and Stephan Kolnsberg†

*† Fraunhofer Institute of Microelectronic Circuits and Systems (IMS)

Finkenstr. 61, D-47057 Duisburg, Germany

* Email: thomas.stuecke@ims.fraunhofer.de

Telephone: (+49) 203-3783-258, Fax: (+49) 203-3783-153

Abstract—The designer of practical receivers must deal with several problems in the analog as well as in the digital part. All these undesired effects have a large impact on the system performance, which is commonly described in terms of bit error rate (BER) or packet error rate (PER). In various textbooks, the theoretical relation between E_b/N_0 and BER is only given for an assumed perfect receiver system. However, the theoretical equations are not capable to predict the performance of a system in presence of an interferer or non ideal components correctly. Instead, a system simulation is necessary. In this contribution, a model of the analog front-end (AFE) will be introduced, which describe several effects which can occur. This model can be integrated in a flexible system simulator and can be used to determine and to verify specifications of the whole front-end or of its single stages. Simulation results are presented, which reveal that simple assumption made in common theory did not hold.

I. INTRODUCTION

There are various wireless communication systems for private and industrial use. To design such a complex wireless system successfully, it is crucial to perform an appropriate system level design at an early stage of the design process. Several parasitic effects of a practical system must be considered in this system level design step.

A practical receiver must cope with noise, non-linearity of its stages, and - depending on the used architecture - with DC offsets and/or I/Q mismatch as well as limited stopband damping of filters. There are different origins for non-linearity in circuits, which cause problems as harmonics, gain compression, desensitization and blocking, cross modulation and intermodulation. Noise occurs as thermal noise and 1/f noise and can also couple into the signal path as phase noise [1].

The following considerations in this paper are based on the direct-down receiver depicted in Fig. 1. This is well suited for a low power receiver [2] and thus especially for ZigBee.

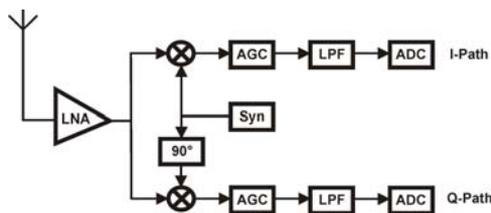


Fig. 1. Receiver architecture.

There are different origins for non-linearity in circuits [3], [4]. As a first order model for such receiver, we assume only a non-linear, memoryless system. The signal passing through the front-end can be described using a Taylor series approximation [1], [4], [5]

$$y(t) = c_1 \cdot x(t) + c_2 \cdot x^2(t) + c_3 \cdot x^3(t) , \quad (1)$$

where $x(t)$ denotes the input, $y(t)$ the output, c_n the Taylor coefficients and all non-linearities with an higher order than three are neglected.

A very simple concept to pursue this approximation is to assume a sum of sinusoids as input signals

$$x(t) = \sum_{k=1}^K A_k \cdot \cos(\omega_k t) , \quad (2)$$

where A_k are constant amplitudes [1], [5]. This simple model leads to handy expressions for signal amplitudes in the receiver and various effects can be predicted: For instance, a single sinusoid with an amplitude A_1 at ω_1 undergoes a gain reduction if accompanied by another sinusoid with amplitude A_2 at ω_2 - called desensitization or in worst case blocking. Theory predicts, that the output signal would be

$$y(t) = c_1 \cdot \left(1 - \frac{3}{4} \left| \frac{c_3}{c_1} \right| A_1^2 - \frac{3}{2} \left| \frac{c_3}{c_1} \right| A_2^2 \right) A_1 \cdot \cos(\omega t) + \dots . \quad (3)$$

However, the gain reduction due to the term in brackets in (3) can not explain the performance degradation experienced in practice, especially in the case of only a single interferer.

For an accurate prediction several practical issues have to be considered. 1. Received signals are never sinusoids. They have a spectral extension and hence intermodulate with themselves causing disturbance of the desired signal band. 2. There is aliasing at the analog-to-digital converter (ADC) interfacing the analog and the digital front-end (DFE). 3. The aliasing strongly depends on the filter preceding the ADC. 4. Actual digital receiver implementations differ from theoretical prototypes due to finite word width, lack of perfect synchronization, and further aspects.

An unknown influence of the AFE on system performance may mislead the system designer into too tough noise and linearity specification. This results in a too high receiver

power consumption, since the noise figure (NF) and the input-referred third-order intercept point (IIP3) is tied up with it [2]. Therefore, a system simulation is absolutely essential to evaluate the resulting performance of the whole system and to help e.g. to optimize the power consumption of the whole receiver.

This paper is structured as follows: Section II discusses the influences on the BER performance of the receiver. The modeling of the system is explained in Section III and simulation results are presented in Section IV. Finally, conclusions and outlook are given in Section V.

II. BER PERFORMANCE OF RECEIVERS

The BER performances of receivers are affected by several undesired effects. To appraise their impact on the simulation results, in this Section approaches are shown.

A. Theoretical $\frac{E_b}{N_0}$ Necessary at Demodulator Input

The ZigBee standard [6] specifies the receiver sensitivity as the smallest input power measured at the antenna terminal which yields to a PER (packet error rate) less than 1% , without the presence of an interferer. The bit errors are assumed as equally distributed and uncorrelated. Since the BER is easier to compute from the SNR, PER must be converted into BER by $BER = 1 - (1 - PER)^{\frac{1}{N}}$, where PER is the packet error rate and N is the average number of relevant bits in a packet. According to the ZigBee standard [6], we assume 20 octets of the PSDU (physical layer service data unit), 1 byte start-of-frame delimiter plus 7 bits decoding the frame length. This gives $N = 175$, resulting in a $BER < 5.74 \cdot 10^{-5}$.

According to [7], [8] the theoretical BER of a DBPSK system can be expressed by (4). Since ZigBee uses DBPSK modulation at 868 / 915 MHz, the theoretically necessary $\frac{E_b}{N_0}$ can be calculated using (5).

$$BER = 0.5 \cdot e^{-\frac{E_b}{N_0}} \quad (4)$$

$$\left. \frac{E_b}{N_0} \right|_{Demod} = 9.58 \text{ dB} \quad (5)$$

B. $\frac{E_b}{N_0}$ at the Antenna

A further important figure is the theoretical $\frac{E_b}{N_0}$ at the antenna. With a AWGN channel model and an assumed perfect receiver (without any negative impact to received signal and noise) with a matched filter, the $\frac{E_b}{N_0}$ at the antenna of the receiver can be computed as

$$\left. \frac{E_b}{N_0} \right|_{Ant} = \frac{\frac{1}{T_B} \int_0^{T_B} |s(t)|^2 dt}{\frac{1}{T_B} N_0} = \frac{P_{Sig}}{kT \cdot B} \cdot SF \quad (6)$$

with absolute temperature T expressed in Kelvin, Boltzmann constant k and according to [6] signal power $P_{sig} = -92$ dBm (receiver sensitivity), bandwidth of the ZigBee signal $B = 300$ kHz and the spreading factor $SF = 15$. This yields at the antenna to an

$$\left. \frac{E_b}{N_0} \right|_{Ant} = 38.96 \text{ dB} \quad (7)$$

However keep in mind, this represents the ideal case only. Another channel model, e.g. a Rayleigh fading channel will degrade the $\frac{E_b}{N_0}$ significantly.

C. $\Delta \frac{E_b}{N_0}$ - The Design Margin

The $\frac{E_b}{N_0}$ at the antenna is larger than the one, which is necessary at the input of the demodulator. Both are depicted in Fig. 2. This gives a margin $\Delta \frac{E_b}{N_0}$ for the system design of the stages in between. It can be calculated as

$$\Delta \frac{E_b}{N_0} = \left. \frac{E_b}{N_0} \right|_{Ant} - \left. \frac{E_b}{N_0} \right|_{Demod} = 29.38 \text{ dB} \quad (8)$$

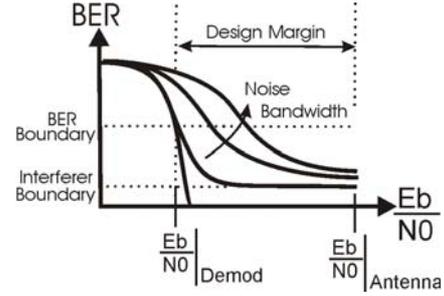


Fig. 2. Distribution of the $\frac{E_b}{N_0}$.

It is very tempting to exploit this margin completely for the noise figure of the receiver. However, it must be shared between the analog and digital front-end. In the analog part e.g. noise, non-linearity in circuits, I/Q mismatch and DC offsets, and in the digital part algorithms as synchronization (carrier frequency, chip and frame) exhaust the quota. Therefore, $\Delta \frac{E_b}{N_0}$ describes the loss of the $\frac{E_b}{N_0}$ along the receiver chain.

D. Impact Equivalent Noise Bandwidth of Filters

Normally in theory BER vs $\frac{E_b}{N_0}$ are derived assuming a matched filter. Since ZigBee uses raised cosine pulse shaping, the received signal contains only energy in a limited bandwidth.

A suitable view point is the assumption, that only the equivalent noise bandwidth of the antialiasing filter effects the SNR. This approach is comparable to the system example in [9] with a non-return to zero signal and a raised cosine receive filter. As long as the filter bandwidth in the receiver is larger than the signal bandwidth, the received signal can be assumed as unaffected. In contrast, the equivalent noise bandwidth is increased to B_{eq} given by (9) according to [4], where H_{pk} is the peak value of the magnitude of the filter transfer function $H(f)$.

$$B_{eq} = \frac{1}{|H_{pk}|^2} \int_0^{\infty} |H(f)|^2 df \quad (9)$$

The result of this is the modified (5) which can be rewritten as (10). Thereby, the curves in the BER diagram will be shifted to higher $\frac{E_b}{N_0}$ values see Fig. 2.

$$\left. \frac{E_b}{N_0} \right|_{Demod, B_{eq}} = \left. \frac{E_b}{N_0} \right|_{Demod} - 10 \cdot \log_{10} \left(\frac{B_{eq}}{Hz} \right) \quad (10)$$

E. BER Performance in Presence of an Interferer

A presence of an interferer also has a great impact on the BER system performance. To assess the influence, it may be suitable to assume, that only the noise figure and the interferer degrade the performance. With a comparable approach as for (6) result (11). Case differentiation for the interferer assumed as a ZigBee signal and a non ZigBee signal is necessary.

$$\frac{E_b}{N_0 + E_{Int}} \Big|_{Demod} = \frac{\int_0^{T_B} |s(t)|^2 dt}{N_0 + \int_0^{T_B} |s_{Int}(t)|^2 dt} \quad (11)$$

As a result, a strong interferer, together with a finite filter attenuation, introduces a lower BER boundary depicted in Fig. 2.

III. SYSTEM MODEL AND SIMULATION

The simulation is carried out in the time domain. However, a problem must be solved: The RF-signal bandwidth is 3 decades lower than the carrier frequency. According to Nyquist, the computation step rate must be more than twice of the highest frequency. The high sampling rate yields a long simulation time, especially if time consuming BER curves shall be evaluated. Therefore, an adequate baseband model is absolutely crucial, to avoid unacceptable simulation times.

The model can be partitioned into different parts as depicted in Fig. 3. It includes the equivalent baseband model of the AFE non-linearity and I/Q mismatch (ANM), the DC offset, a low pass filter (LPF), an adequate noise generation, and the digital part. The ANM block also include an upsampling, which is necessary for two reasons: At first, after the direct down conversion, the interferer is located at a higher frequency than the desired signal. Thus, the interferer signal in the model must be shifted to a center frequency corresponding to the RF channel spacing. At second, the analog filter is approximated by a digital Matlab filter. Therefore, the sampling rate must be increased as well, to represent the filter slope in an appropriate way (Noise is also shaped by this filter). All parts of the model are embedded in a simulation environment to derive specifications for the analog and for the digital part and to verify e.g. simulation results from the circuit simulations.

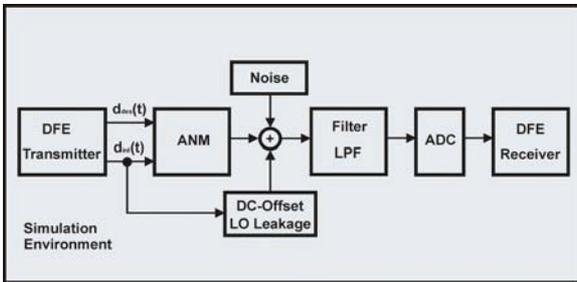


Fig. 3. Block diagram of the simulation environment, including the equivalent baseband model of the AFE non-linearity and I/Q mismatch (ANM).

A. Digital Part (DFE)

The digital part (DFE) of the receiver, which represents the digital part of the physical layer PHY, includes a carrier frequency-, a chip- and a frame-synchronization, preprocessing of the chips, despreading, and transfer of the received data to the medium access layer (MAC). The digital front-end of the transmitter picks up the data from the MAC layer, spreads the bits and applies a raised cosine filtering. A more detailed description is given in [6], [10].

B. Input Signals - Desired and Interferer

The desired signal and the interferer are modeled as ZigBee signals, where the interferer is located at an adjacent channel and is synchronized with the desired signal. This is a worst case situation. Both signals are pulse shaped by a raised cosine filter and are applied as baseband signals to the input of the ANM building block as $d_{des}(t)$ and $d_{int}(t)$ as depicted in Fig. 3.

C. I/Q Mismatch and Down Conversion

The I/Q mismatch can be modeled as shown in Fig. 4. This model also includes the down conversion function of the mixer, where α_I and α_Q denote the different gain in the I- and Q-path, ω_0 is the LO frequency of the mixer and φ_{mis} describes the deviation from the perfect 90° phase shift of both LO signals.

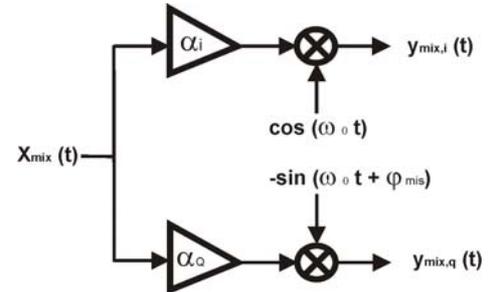


Fig. 4. Model of the I/Q mismatch and down conversion mixer.

The complex output signal $y_{mix}(t)$ is sum of the I and Q outputs as given by (12). A perfect complex down conversion is simply a multiplication of the input signal by $e^{-j\omega_0 t}$, i.e. a complex harmonic oscillation with negative frequency. A complex down conversion in presence of an I/Q mismatch (i.e. $\alpha_I \neq \alpha_Q$, $\varphi_{mis} \neq 0^\circ$) can be modeled by adding a disturbance to the perfectly down converted signals. The disturbance is proportional to the input signal multiplied by a complex harmonic oscillation of positive frequency. In (15) the output signal of the imperfect down converter is expressed in terms of $\underline{\alpha}$ and $\underline{\beta}$ which are easily computed from α_I , α_Q and φ_{mis} . In the ideal case $\underline{\beta}$ is zero and $\underline{\alpha}$ is unity.

$$y_{mix}(t) = x_{mix}(t) [\alpha_I \cdot \cos(\omega_0 t) - j\alpha_Q \cdot \sin(\omega_0 t + \varphi_{mis})] \quad (12)$$

$$\underline{\alpha} = \frac{1}{2} (\alpha_I + \alpha_Q \cdot e^{-j\varphi_{mis}}) \quad (13)$$

$$\underline{\beta} = \frac{1}{2} (\alpha_I - \alpha_Q \cdot e^{+j\varphi_{mis}}) \quad (14)$$

$$y_{mix}(t) = x_{mix}(t) [\underline{\alpha} \cdot e^{-j\omega_0 t} + \underline{\beta} \cdot e^{+j\omega_0 t}] \quad (15)$$

D. Output ANM of the Block

For the calculation of the output signal, the following input signal is considered

$$x(t) = \text{Re} \{ A_{des}(t) \cdot e^{j\omega_{des}t + j\varphi_{des}} + A_{int}(t) \cdot e^{j\omega_{int}t + j\varphi_{int}} \} \quad (16)$$

with $A_{des}(t) = \hat{u}_{des} \cdot d_{des}(t)$ and $A_{int}(t) = \hat{u}_{int} \cdot d_{int}(t)$. The input signal consist of the two baseband signals, the desired one $d_{des}(t)$ and the interferer $d_{int}(t)$. The factors \hat{u}_{des} and \hat{u}_{int} are used to adjust the input signal amplitude to the corresponding received signal power.

The output signal $y_{ANM}(t)$ of the ANM building block can be computed assuming the input signal of (16), the description of a non-linear device (1), and the model of the I/Q mismatch (15)

$$y_{ANM}(t) = \sum_{m=1}^M \underline{\alpha} [y_m(t) \cdot e^{j\omega_m t + j\varphi_m}] + \underline{\beta} [y_m(t) \cdot e^{-j\omega_m t - j\varphi_m}] , \quad (17)$$

where m denote the number of the regarded harmonic and intermodulation product, down converted to baseband.

All stages of the receiver are tuned to the desired signal. Therefore, they provide relatively narrowband amplification and the signals which are too far away from zero frequency can be neglected.

E. Modeling of Noise

It is important to deal with a proper modeling of noise. It can be asserted with sufficient accuracy, that the antenna receives white noise. Equivalent to the derivation in [11], the noise can be modeled as two statistically independent noise sources in the I- and Q-path (power spectral density is twice of the antenna).

The easiest way to generate band limited noise is to use the antialiasing filter model itself. The noise can be generated as white noise (sufficient high sampling rate) and scaled by the noise factors of previous stages, before being applied to the input of the filter together with the ANM output signal.

F. DC Offset

To model the effects of DC offset, it is necessary to assess or to measure the RF isolation of the LNA input and the mixer RF input to the LO input of the mixer. These effects can be modeled as a constant DC signal and a fraction of the squared interferer signal (with center frequency at zero), which can be added to the other signals at the input of the LPF - filter.

G. LPF - Filter and ADC

The low pass filter preceding the ADC accomplishes two tasks. The first is to avoid aliasing effects by the sampling inside the ADC. According to Shannons sampling theorem, it is necessary, to limit the signal bandwidth to half of the sampling frequency. The second task is the channel selection which can be carried out either in the digital or in the analog part. This is possible by a proper choice of the filter bandwidth.

The ADC itself is realized as a Matlab-code which is used as a function in the receiver simulation.

IV. SIMULATION RESULTS

In this Section several simulations results are presented. To clearly show the influence of the analog part on the BER performance of the receiver, all simulations were performed with the digital part assumed as perfect. To neglect the effect of quantisation noise, an adequate bit resolution is used. The antialiasing filter has a high order to suppress the interferer sufficiently.

At first we compare our model of the receiver chain, setting different 3-dB corner frequencies of the antialiasing filter (150, 290, 370 and 800 kHz), with the theoretical curve of DBPSK depicted in Fig. 5. The filter is realized as a 7th order Butterworth low pass filter. These results are obtained without the presence of an interferer. The BER curve for the 150 kHz antialiasing filter is almost identical to the theoretical BER curve of DBPSK. However, this choice results in an unpractical receiver design limited by the typical large process tolerances in CMOS technology. Thus, the 290 kHz filter seems to be a good compromise.

Fig. 6 shows the simulation result with a 290 kHz filter. The theoretical DBPSK curve can be fitted to theoretical one by a constant factor (Section II) based on the equivalent noise bandwidth of the filter. Obviously, both curves are very close together and are taken as a reference for the following plot.

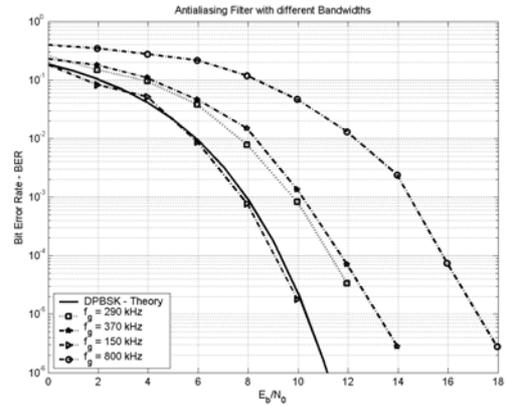


Fig. 5. Different filter bandwidth of antialiasing filter.

To determine the impact of an interferer, a strong one of -29 dBm with the same spreading factor is assumed additionally now. The result is depicted in Fig. 7. Although an linear receiver is assumed, the curve starts to deviate at

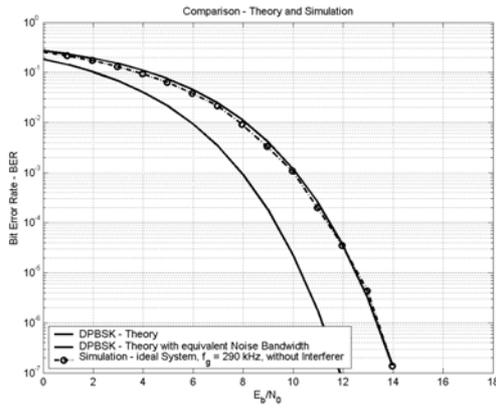


Fig. 6. DPBPSK theory with equivalent noise bandwidth and simulation result.

$BER \approx 3 \cdot 10^{-4}$. Since the antialiasing filter is not a brickwall filter, the attenuation of the interferer is finite. This yields to aliasing effects after sampling of the signal inside the ADC and thereby to a degradation of the BER performance. Thus, the efficiency of the antialiasing filter and the power of the interferer determines the lower achievable BER boundary value.

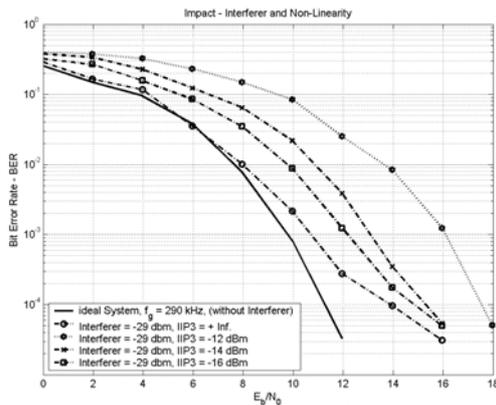


Fig. 7. Impact of the interferer and the non-linearity.

If a non-linear behavior of the receiver chain is supposed (finite IIP3), the BER curve is shifted towards higher $\frac{E_b}{N_0}$ values. In this case, depicted in Fig. 7, a higher $\frac{E_b}{N_0}$ is required to comply with the specified BER boundary. For example this yields to a severer specification for the receiver NF. These simulation results reveal, that the simple assumption made in common theory did not hold.

V. CONCLUSION AND OUTLOOK

In this paper, a model of the analog front-end is presented, which describes the behavior of a radio receiver at the system level.

The theoretical $\frac{E_b}{N_0}$, which is necessary to comply with the ZigBee standard [6], has been derived. Additionally, it has been shown, that the consideration only of desensitization and

blocking, leads to wrong conclusions for the system level design.

The system simulation shows precisely the influence of the different factors to the whole system performance. Therefore, it is possible to evaluate directly the resulting BER curve of the considered receiver system. For example, the presence of an interferer at the input of a non-linear front-end can be simulated and the influence of a practical antialiasing filter as well. With the assistance of the simulator it is possible to derive and to verify specifications for the single receiver stages. The system simulator can also be used to develop algorithms for the digital front-end like carrier frequency-, chip- and frame-synchronization and for performance tests. Therefore, an analog and digital co-design is supported.

The model will be extended by generation of phase noise and $1/f$ noise. Furthermore, the desired signal and the interferer can be implemented with varying signal power and an algorithm simulating the function of an AGC. With respect to the used frequency band, it will be useful to model a GSM, UMTS, Bluetooth, RFID or a WLAN signal as an interferer. If for example the target application is a sensor network in an industrial environment, particular interferers have to be considered. The current model assumes a simple AWGN channel. Thus, it will be advantageous to implement a more realistic channel model, e.g. a special indoor channel model.

In summary, the level diagram provides just a helpful short overview while the system simulation considers the impact of many effects in the analog and digital part and thus forms a good basis for a successful radio level transceiver design.

REFERENCES

- [1] B. Razavi, *RF Microelectronics*, 1st ed. Cambridge, New York, Melbourne, Madrid, Cape Town: Cambridge University Press, 1998.
- [2] A. Abidi, G. Pottie, and W. Kaiser, "Power-Conscious Design of Wireless Circuits and Systems," *Proceedings of the IEEE*, vol. 88, no. 10, pp. 1528–1545, 2000.
- [3] J. Janssens and M. Steyaert, *CMOS Cellular Receiver Front-Ends*, 1st ed. Boston, Dordrecht, London: Kluwer Academic Publishers, 2001.
- [4] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, New York, Melbourne, Madrid, Cape Town: Cambridge University Press, 2004.
- [5] U. Tietze and C. Schenk, *Halbleiter-Schaltungstechnik*, 11st ed. Berlin, Heidelberg, New York: Springer Verlag, 1999.
- [6] "IEEE Std 802.15.4 -2003, IEEE Standard for Information technology - Telecommunications and information exchange between systems - Local and metropolitan area networks - Specific requirements - Part 15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs)," available in the internet: www.zigbee.org.
- [7] T. Rappaport, *Wireless Communications*, 2nd ed. London, Sydney, Toronto, Mexico, New Delhi, Tokyo, Singapore, Rio de Janeiro: Prentice-Hall, 1999.
- [8] J. Proakis, *Digital Communications*, 4th ed. Singapore: McGraw-Hill, 2001.
- [9] R. Mäusl, *Digitale Modulationsverfahren*, 4th ed. Heidelberg: Hüttig Verlag, 1995.
- [10] J. Gutiérrez, E. Callaway, and R. Barrett, *Low-rate wireless personal area networks - enabling wireless sensors with IEEE 802.15.4TM*, 1st ed. New York: IEEE standards wireless networks series, 2004.
- [11] D. Pozar, *Microwave and RF Design of Wireless Systems*, 1st ed. New York: John Wiley and Sons, 2001.