

# 4-MORE RF Platform, testbed for a MIMO MC-CDMA system

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**Abstract**—This paper summarizes the efforts and achievements within the 4-MORE project, concerning the RF platform development. The design of this MIMO MC-CDMA subsystem as well as its simulation, assembling and performance evaluation results have been included in this report, paying especial attention to the main RF impairments influencing the BB performance.

**Index Terms**—MIMO MC-CDMA, HW Development, Platform evaluation, 4-MORE

## I. INTRODUCTION

While the third generation terrestrial mobile system (UMTS-UTRA) is currently being deployed, there is already a significant research activity towards what is called 4G systems. In order to accommodate future services requiring high capacity, a broadband component is envisioned with a maximum information bit rate of more than 2-20Mbps in a vehicular environment and possibly 50-100Mbps in indoor to pedestrian environments, using a 50-100MHz bandwidth. One of the most promising technologies for this broadband component is Multi-Carrier Code Division Multiple Access (MC-CDMA), which allows combining the merits of OFDM with the ones of spread-spectrum techniques.

At the European level and within the IST Programme, the MATRICE [1] project has undertaken research in order to define and validate access and transmission concepts based on MC-CDMA technology for provision of the broadband component of future mobile cellular systems. The objective of 4MORE project [2] is to complement the MATRICE and worldwide research results, while advancing one step towards implementation though the design of a System on Chip (SoC) for a 4G terminal employing multiple antennas and based on MC-CDMA techniques. The main objectives pursued by this project are to study new communication systems for 4G mobile phone applications based on MIMO MC-CDMA modulations and to propose innovative architectures for mobile terminals parts in terms of modularity, re-configurability, integration and power consumption aspects.

The demonstrator platform will include at least a mobile terminal with 2 antennas and a base station with 4 antennas (4x2). The design and characterization of the RF module, which performs the up conversion of I-Q base-band MC-CDMA signals to the 5GHz band and the other way round, is described in this paper.

The rest of the document is structured as follows: section II includes the design of the RF module, while section III covers the simulation process. In section IV, measurement results are summarised, whereas most relevant conclusions are presented in section V. Finally, section VI deals with future work.

## II. RF MODULE DESIGN

The 4MORE project system will work at 5 GHz, more specifically the 5.150-5.250 GHz band has been selected, since demonstration activities can be carried out in this license free band. Regarding the air interface, MC-CDMA has been adopted so as to reach the challenging data rates of the 4MORE system, to be achieved within a total bandwidth of 50 MHz.

The RF platform of the 4MORE system includes all necessary modules to perform both up and down frequency conversion of the base band data signals to the operation band. There are several possible RF architectures for implementing such a system, however, the pressure to reduce the cost of the RF communication system has driven to develop an architecture with higher level of integration and fewer off-chip components, which has been the reason for selecting a Zero-IF architecture. Indeed, a two step direct conversion has been implemented so as to avoid injection pulling and improving the efficiency with regards to the I/Q matching [3].

The assembly of the RF module involves the design and characterisation of different subsystems to carry out the required functions: modulation/demodulation, frequency synthesis and amplification.

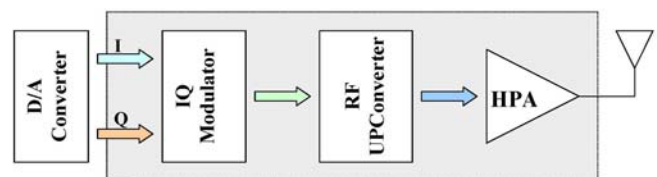


Fig 1.- Transmitter block diagram

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The general block diagram of the RF transmitter is shown in Fig. 1, where the I/Q base band signals are applied to a direct modulator which converts the signal up to 1.2 GHz. Then, a second frequency conversion to the 5 GHz band is carried out.

The ratio between power consumption and transmitted power is the most important trade-off to resolve in the transmitter. Commercially available amplifiers show low power added efficiency (around 30%) which implies high biasing currents and consequently heating problems. Moreover, it must be taken into account the PAPR (Peak to Average Power Ratio) of the MC-CDMA, which means the use of back-off at every device in the system to avoid distorting the signal, leading to a loss of power efficiency. The back-off depends on the linearity of the devices, the more non-linear the device is, the bigger the back-off is necessary to achieve the same distortion levels. These facts have a great influence on the RF systems sizes and weights.

On the other hand, the selected two-step architecture for the receiver is presented in Fig. 2. In this case, a first down conversion from 5 GHz to 1.2 GHz is carried out. After that, a direct conversion from 1.2 GHz to base band is done by the demodulator.

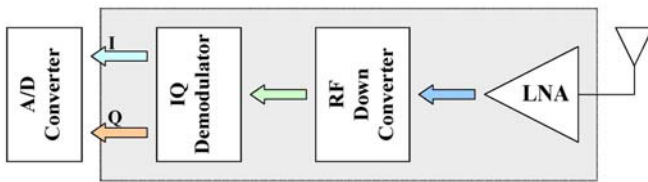


Fig 2.- Receiver block diagram

The receiver has been designed so as to fulfil the required S/N ratio, which implies 7 dB of NF as worst possible case. Another important parameter to take into account is the transfer function of the filters, specially the image frequency rejection.

Both transmitter and receiver share the same antenna, either transmission or reception is selected by a switch, which is controlled from base band through a Sub D-26 connector. A critical parameter to ensure proper operation is the isolation between the transmitter and receiver chains.

The total dynamic range of the RF system is designed to be no lower than 70 dB, divided as follows: the transmitter shows a 30 dB gain control with 0.5 dB steps, whereas the receiver has a 40 dB range controlled by an analogue voltage. These gains are controlled from base band through the formerly referred Sub D-26 connector.

A calibration path (whose block diagram is depicted in Fig.3) has been included in the design of the RF system so as to minimize the overall influence of any potential I/Q channel quadrature phase errors and/or amplitude mismatches. The subsystem operates in the following way: once a calibration base band signal is converted up to 1.2 GHz, using the direct up converter, the calibration path is enabled by a switch,

which permits to send the signal to the direct down converter. Then, the test signal is processed at base band to correct as much as possible the impairments, such as phase and amplitude imbalances. This calibration will be carried out periodically at each transceiver chain of the MIMO RF front-end.

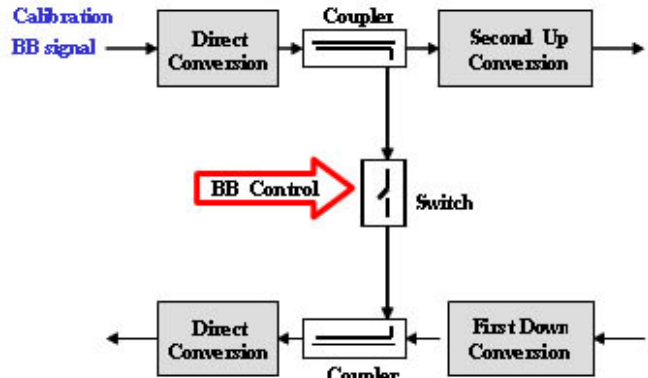


Fig 3.- Calibration path diagram

A critical aspect in the final assembly of the whole RF module is the correct shielding to avoid interference between different devices. The most widespread solution for this problem is the housing, which implies the design and development of specific mechanical boxes, ensuring this way electromagnetic isolation, as well as physical protection.

### III. SIMULATIONS

The ADS© simulation environment from HP Eesof provides access to a number of simulation engines and algorithms through what is referred to as test benches. This simulator offers the implementation of the Circuit Envelope or envelope transient [4] which was developed specifically to efficiently simulate the transient and complex modulated RF signals found in today's wireless circuits [5-6]. The main advantage of the mixed frequency/time domain approach at the base of circuit envelope is that it considers a modulated signal as a combination of low frequency dynamic- the envelope of the carrier or the modulation, analyzed with transient-, and a high frequency dynamic- the carrier, analyzed with harmonic balance (HB)- and performs the simulation only in the relatively narrow frequency band that is occupied by the modulated signal. Therefore, two different time scales are considered. Unlike transient analysis, it does not need to analyze the complete spectrum up to the maximum frequency set by the simulation period. This results in an enormous time saving when trying to reach the necessary results.

Envelope transient technique is the best suited and the only practical simulation technique, used in conjugation with harmonic balance (HB) and linear RF simulation, for all present and future wireless communication designs. One of its most useful applications, from the designer point of view, is predicting the response of a circuit when is driven with a complex digital modulation which cannot be performed with

quasi-periodic harmonic balance. It can also analyze periodic signals spectra with their discrete spectral lines, such as those representing the inter-modulation products from a mixer or amplifier under multi-tone sinusoidal excitation more efficiently than HB as the frequency offset between tones decreases.

ADS HB tool has been used in order to simulate the performance of both transmitter and receiver chains due to its fast, memory efficient matrix algorithms for the quasi-periodic steady-state analysis of circuits.

As an example of the envelope transient simulations carried out, in Fig.4 the result of the two tone third order intermodulation simulation for the RF receiver is shown. Two pure tones of -39dBm power amplitude each, with a frequency offset of 5 MHz have been introduced to the receiver, obtaining a total output power of -10dBm and a carrier to intermodulation ratio (C/I) of 60.8 dBc.

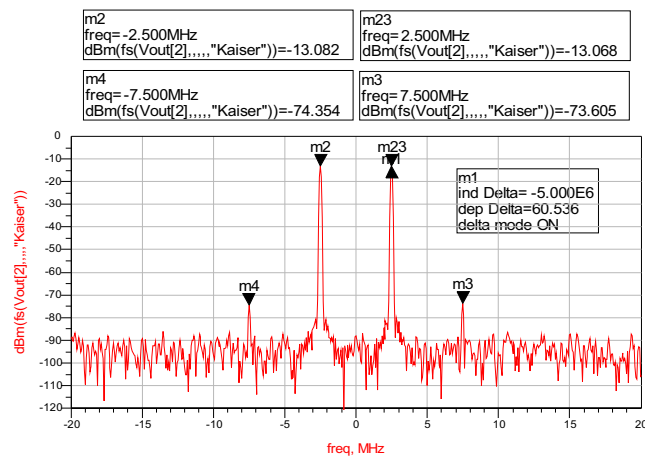


Fig 4.- RF receiver two tone third order intermodulation level simulation

Concerning some of the values required for the link budget calculations, the simulations offered a NF value of 5.3 dB, while maximum transmitted power reached 16.8 dBm at the HPA output. Nevertheless, the transmitter 1dB output compression point ( $P_{1dB-Out}$ ) value of 25.8 dBm advises paying special attention at the PAPR characteristics of the MC-CDMA signal, in order to guarantee the highest linearity, and hence, the lowest distortion, in the transmission.

#### IV. MEASUREMENTS

Once the assembling process has been completed, it is time to test all the sub-blocks before the final integration. Since there will be a presentation of the main transceiver performance values, only two submodule results will be included in their stand-alone previous evaluation: the DC power supply and the oscillators.

The first section of the transceiver analysis was covered by proper consumption verification and normal temperature operation, whose values were successfully matched to the design ones.

#### A. DC Power supply

The device employed to convert the usual 110/220 V 50/60 Hz AC signal to the different DC voltages (positive and negative), required to bias the RF circuitry, will be presented in this section.

Apart from the voltage values, their ripple is a critical figure of merit which has to be carefully minimized, due to the dependence of the Oscillator Phase Noise on this parameter (Oscillator DC bias supply showing high DC ripple levels causes bad oscillator phase noise performance). Bearing in mind the above mentioned considerations, a fully integrated, high efficiency switching DC Power supply has been designed, assembled, tested and integrated. The main characteristics of this power supply are summarised in Table I.

Table I.- DC Power supply

Voltage Value	Ripple	Maximum Current	Real consumption
+5	Negligible	10 A	2.35 A
+9	Negligible	2 A	0.08 A
-5	Negligible	2 A	0.04 A

Besides, protection mechanisms have been introduced so as to ensure that no positive voltage supply is provided to the RF components before its correspondent negative one had been supplied.

The second stage included the oscillator analysis, specially their phase noise behaviour, for it being one of the most critical RF impairments to be faced by BB correction algorithms [7].

#### B. Oscillators

Following the testbed spirit of the project, the local oscillators has been designed employing a TCXO (Temperature Controlled Xtal Oscillator) PLL (Phase Locked Loop) frequency reference, and the values of the phase noise, for both PLOs (Phase locked Oscillator), measured.

The higher the frequency is, the stronger the influence on the phase noise it has. For this reason, the values obtained after the phase noise characterization, for the most representative offset frequencies of the 4 GHz PLO, appear in Table II.

Table II.- PLO Phase Noise Measurement

Frequency Offset	Phase Noise Level (Measured)
10Hz	-60 dBc/Hz
100Hz	-70 dBc/Hz
1KHz	-80 dBc/Hz
10KHz	-88 dBc/Hz
100KHz	-110 dBc/Hz
1MHz	-120 dBc/Hz

It has been proved [8] that phase noise values corresponding to frequencies smaller than  $0.1 \cdot \Delta f$  (10% of the subcarrier spacing), should not have influence over the system if there is

channel estimation. This way, for the final number of subcarriers,  $N_s$  (still undefined within the project), in our 50 MHz signal bandwidth, we could obviate the phase noise values for offset frequencies lower than  $5/N_s$  MHz.

### C. Overall Transceiver Performance

As explained in the beginning of this section, once all the submodules were individually tested and correctly assembled, the transceiver is ready to be evaluated.

A critical aspect in the final assembly of the whole RF transceiver is the design and manufacture of the housing where the RF electronics will be placed. In this sense, an enclosure EMC compliant has to be developed, ensuring system robustness as well as input and output signals accessibility in an easy way. According to this, a 19 inches standard metallic rack is used to house the transceiver. Inside this rack, the transmitter and receiver modules, the DC power supply and the distribution board (controlling the calibration path) are located. Figure 5 shows the front view of the transceiver rack, after the integration was completed.



Fig 5.- Front view of the transceiver's rack

The transceiver evaluation was split in the down-stream chain and the up-stream one, namely, receiver and transmitter. Besides, the proper isolation and switching behaviour between both operation modes were also examined.

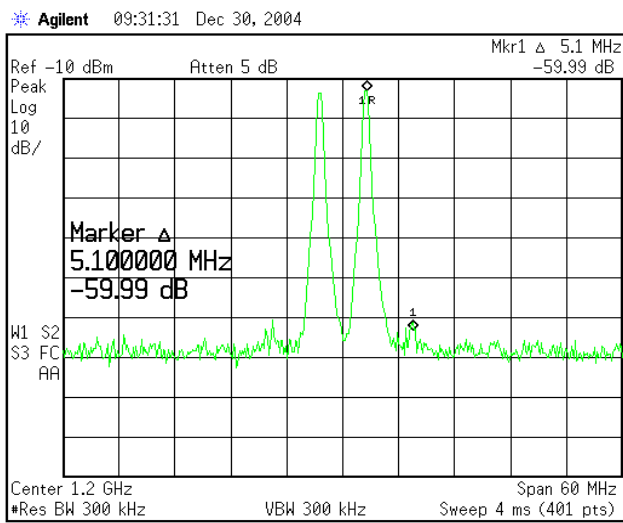


Fig 6.- RF receiver two tone third order intermodulation level measurement

In order to test the receiver linearity over the input power operation range, the well known Two Tone Test has been carried out by applying two pure sinusoidal input tones to the receiver. The power level of the obtained output tones is -13 dBm each (-10 dBm total power received) with a frequency spacing between tones of 5 MHz. With these conditions, the power level of the third order intermodulation products at the receiver output is -73 dBm, as shows Fig.6, leading to a carrier to intermodulation figure of merit at the output (C/I) of 60dBc, really close to the value resulted from the simulation process.

As a summary of the receiver performance evaluation, the following relevant parameters, among others, have been also measured: gain ( $G=25$ dB), noise figure ( $NF=6.75$ dB), ripple (1dB over the whole band), 1 dB output compression point ( $P1dB_{out}=11$ dBm), minimum detectable signal -100dBm. The isolation between transmitter and receiver is 68dB, while the matching values were  $S_{11} < -15$  and  $S_{22} < -12$ .

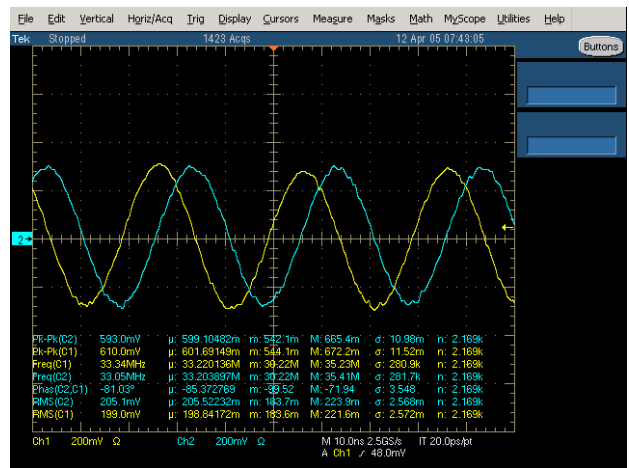


Fig 7.- I/Q capture at 30 MHz from a 5.23 GHz test tone

The second part of the transceiver evaluation is, obviously, that concerning the Up-stream chain. The characterization of the RF transmitter results in obtaining as most representative parameters: a 36dB gain, with a maximum ripple of 0.9dB, whereas the measured 1dB output compression point ( $P1dB_{out}$ ) reached a value of 20.71dBm.

Measurements of EVM, magnitude and phase error have been also performed for the full transmitter chain in order to check if the obtained results are compliant with the 3GPP standard [9].

The conclusion from Fig.8, where these results appear, is that the 3GPP standard is fulfilled, not only with regards to the maximum allowed EVM -12.8% (which can be reduced to 10% by a slight modification in the calibration path architecture) versus the 13% appearing in the standard – but also the frequency mask considering the spurious elements and the ACPR requirements.

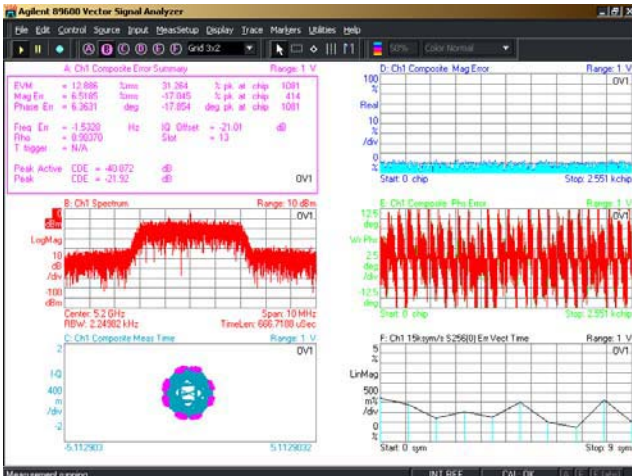


Fig 8.- Part of the 3GPP standard fulfillment verification

## V. CONCLUSIONS

A complete presentation of the 4MORE RF platform has been carried out, including not only the description of the designs, but also the measurements of the developed boards and boxes.

From the presented work some conclusions can be extracted. The Zero-IF direct conversion for MC-CDMA is tested within a MIMO testbed platform. The results, matching the design and the powerful simulation tools values, provide a positive feedback for the designers.

## VI. FUTURE WORK

Future work is required in the completion of the whole multiple antennas RF front-end, including the integration with the antennas and the common BB platform, with which the demonstration platform development will be concluded.

## VII. ACKNOWLEDGEMENTS

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