Pipelining Architecture Design of the H.264/AVC HP@L4.2 Codec For HD Applications

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Abstract : This paper presents the macroblock/slice level pipeline structure for an H.264/AVC HP@L4.2 codec. In H.264/AVC, level 4.2 (L4.2) in high profile (HP) describes the encoding/decoding capability of 1920x1088@64p sequence/bitstream of up to 62.5 Mbps. To meet this tremendous specification, the novel hardwired architecture of the H.264/AVC codec is also presented. It supports both encoding and decoding and shares commonly used hardware modules. In our system, the video subsystem including the H.264/AVC codec is classified into four principle functions: video coding, memory management, reference cache-buffer control, and top control. With regard to H.264/AVC processing, the video coding function comprises eight modules. These modules are arranged as a six-stage macroblock pipeline for the encoder and a four-stage macroblock pipeline for the decoder. With the proposed schemes adopted, a software C model and an FPGA platform were developed for verification. The simulation results indicate that our design approach successfully performs the real-time encoding/decoding of the H.264/AVC HP@L4.2 sequence/bitstream at an operating frequency of 266MHz.