New LZW Data Compression Algorithm and Its FPGA Implementation

Author(s) : Wei Cui (Beijing Institute of Technology, China)

Abstract : This paper presents a new LZW data compression algorithm that partitions conventional single large dictionary into a dictionary set that consists of several small address space dictionaries. As doing so the dictionary set not only has small lookup time but also can operate in parallel. Simulation results show that the proposed algorithm has better compression ratio for image data than conventional LZW algorithm and DLZW (dynamic LZW) algorithm, has competitive performance for text data with DLZW algorithm. In addition, a parallel VLSI architecture for implementing the new algorithm is proposed, and it is realized using FPGA XC4VLX15–10. The experiment results show that the chip can yield a compression rate of 198.4 Mbytes/s, it is about 6.9 times the compression rate of implementing conventional LZW, and 3.2 times the compression rate of implementing DLZW.