VLSI Architecture of H.264 RDO-based Block Size Decision for 1080 HD

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Abstract:  
Hardware architecture of Rate-Distortion Optimization (RDO) is proposed, which is dedicated to H.264 block size decision of 1080 HD. To achieve high encoding efficiency of H.264, RDO for block size decision is indispensable but suffers from enormous computational costs since distortion and the number of coded bits can be determined only after completing the whole encoding processes of the block. The proposed approach reduces the computational costs by the approximation of bit amount in entropy coding. In addition, four parallel seven stage codec pipeline enables high speed calculation of distortion originated from residual. As a result, the proposed architecture, which can be implemented by 14K gates, achieves real-time processing of HDTV(1920x1080) frames at a rate of 30 fps in 120MHz operation, where 0.5 dB of PSNR is gained in comparison to conventional approaches.