Enabling Ubiquitous Wireless Sensing by a Novel RFID-Based UWB Module

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***Abstract*- In this paper, we present a novel passive CMOS module which uses two different standards in uplink and downlink. It can be used in many applications such as Radio Frequency Identification (RFID), and ubiquitous wireless sensing. Such as conventional RFID systems, the module captures power supply from received RF signal transmitted by a reader and extracts data and clock by using an envelope detector and PIE encoder. However, in uplink instead of back scattering, an Impulse-UWB transmitter is used to improve the system performance and throughput. The UWB communication offers several advantages to the system. A new communication protocol is proposed for the system based on slotted-ALOHA anti-collision algorithm. The module consisting of a power management unit, an RF narrowband receiver, a clock management unit, an IR-UWB transmitter, and a digital baseband are designed in 0.18 CMOS process.**

I. INTRODUCTION

Nowadays, wireless sensor networks (WSN) are widely used in space and environment monitoring. They merge a wide range of information technology that spans hardware, software, networking, and programming methodology. A node in a WSN typically consists of a microprocessor, data storage, radio front-end, analog-to-digital converter (ADC), and sensors. They have limited computational power and can talk to each others and transfer data in a wide area without any central node. They are usually powered by a battery and hence limited life time. To achieve a lifetime of one to five years, the average power consumption must range from 10 to 100μW; while today's commercially available radio transceivers consume typically several tens of mW. To maintain the required power consumption, the nodes must sleep most of the time. This can be realized using low duty cycle operation time such as a 1% or 0.1% duty cycle. [1]

In many applications such as asset monitoring, tracking and positioning no such high performance system with high capacity is needed. In such applications communication between nodes is not necessary and a central base station can retrieve data from the nodes. On the other hand, in these applications, size, price, and lifetime of the module are more important. Having a passive module such as RFID can be a smart solution. Recently, RFID based ubiquitous sensing systems are widely interested [2]. An RFID system identifies the unique tags' ID or detailed information saved in them, which are attached to objects. They are widely used in asset monitoring, access control, supply chain, and many other applications. Passive tags derive the required power from a reader using either inductive coupling or electromagnetic capture and communicate by utilizing load modulation or electromagnetic backscatter [3]. For backscatter passive tags, the returned signal power scales, unfortunately, as the inverse fourth power of the distance to the tag. Therefore, it is difficult to detect them at great distances. On the other hand, backscattering RFID systems suffer from several disadvantages. They are sensitive to interference, multi-path fading, multi-user interference and collision problem, and it is susceptible to passive and active attacks. Therefore, they are not suitable for new applications of RFID which require higher data rate, longer operation range and faster processing speed.

Ultra wideband (UWB) techniques using impulse radios has the possibility of achieving high throughput, long operating range, low power consumption, positioning, ranging and low cost implementation [4]. In this paper we present a self-powered CMOS RFID-Based module which utilizes UWB communication scheme in uplink from tag to reader instead of backscattering. It mainly includes a power scavenging unit, a low power RF receiver, a clock generator circuitry, an ultra-low power impulse UWB transmitter, and a digital baseband controller. A new pipelined communication protocol with enhanced slotted-ALOHA anti-collision algorithm is presented. The final module is designed in 0.18um CMOS technology.

II. SYSTEM DESCRIPTION

A. *System Architecrure*

Figure 1 shows the proposed system concept. The module captures the required power from the environment sources and stores in a storage capacitor. The source can be electromagnetic wave, solar energy, thermal energy or vibration. In this work such as conventional RFID the electromagnetic wave transmitted by a base station is utilize. A voltage sensor circuit senses the capacitor voltage and switches the chip on when there is enough voltage (e.g. 2.5V) and the module starts to operate. While the chip is working, voltage over the storage capacitor is degraded. Therefore, a low-drop-out (LDO) voltage regulator is utilized to provide regulated voltage for the module. If the capacitor voltage becomes less than certain value (e.g. 1.8V), the voltage sensor switches off the chip, and the module starts to gather energy for next run. In such system the module should be able to operate and transmit data in a short time along with low power consumption as less as possible. On the other hand, the data rate should be high while the power consumption is low. Commercially available high data rate transceivers consume much power which is not suitable for such operation.

UWB communication using impulse radio has the possibility to achieve high data rate with low power consumption. Unfortunately, UWB receivers are usually very complex and consume much power, which are not possible to use it in such passive module. On the other hand, the required data rate from the base station to the tag is very low. Therefore, for the downlink from base station to the tag, such as conventional RFID system, the transmitted electromagnetic wave is utilized to carry data.

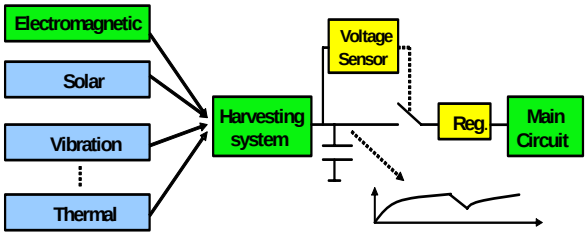


Figure 1. Block diagram of the system concept

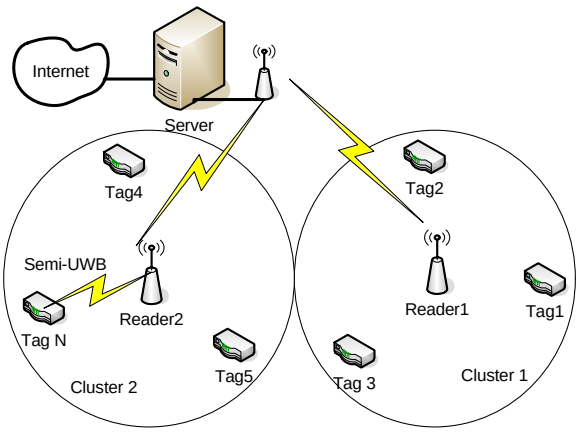


Figure 2. Generic sensor networks architecture.

UWB communication brings several advantages and improvements for the system including of:

- Low complexity on circuit level, and low cost
- Low power consumption
- High processing gain
- Small fast fading margin
- Ranging and positioning capability
- Propagation and interference rejection
- Low probability of detection,
- Multiple access
- Adaptive data rate

An example of a wireless sensor network using asymmetric wireless links is shown in Figure 2. The network consists of hundreds, or thousands of tags divided in several clusters. Each cluster includes all tags in the reading field of a reader (around 10 meters). A reader in each cluster provides power supply for the tags and sends command, data, and synchronization clock using a narrowband RF signal. The tags gather data from an attached sensor autonomously, and pass this data to the correspondent reader through an UWB link, and the reader forwards data to the sensor network server through a Wireless Local Area Network (WLAN). The reader's WLAN interface provides ad-hoc functionality and in case of range or throughput limitation data can be transferred via neighboring nodes.

B. Communication Protocol

A new communication protocol is needed for the proposed system with asymmetric wireless links. Hereby, we introduce a novel baseband protocol focusing on low power consumption budget, robustness, reliability, and network throughput. It performs several functions such as Wakeup, Request, Write, Modify, and Kill. A frame is divided to several time slots and each tag chooses a time slot randomly to transmit data to the reader. Figure 3 shows the data process in two following frames. After receiving the REQ command all tags in the reading area send their ID based on a pipelined protocol. It employs Frame Slotted ALOHA algorithm as the anti-collision protocol. Each tag transmits its ID to the reader in a randomly selected slot of a frame and listens for an acknowledgment (ACK) response during the next slot. When the reader receives and identifies an ID without any collision, sends an ACK in the next slot. The identified tags go to the halt state after receiving the ACK, in order to decrease the collision. Collided tags resend their ID in the following frames in a new randomly selected slot, until all tags are identified. [5,6] By using dynamic frame size allocation and idle slot skipping method, simulation results of the system performance shows that more than 1000 tags can be processed within 500ms. [6]

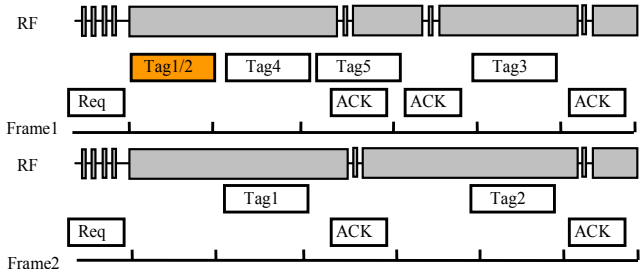


Figure 3. Proposed pipeline protocol for UWB-RFID

III. CIRCUIT IMPLEMENTATION

Circuit implementation issues have been considered in order to achieve the desirable properties of the asymmetric transceiver for the sensor nodes as well as to verify the proposed system architecture. 1.8V 0.18um analog/mixed-signal CMOS technology is selected for the implementation. ISM 900MHz frequency band is used for the downlink and I-UWB transmitter for the uplink. Figure 4 shows the detailed block diagram of the module. It includes a power management unit, a narrowband RF receiver, a clock generator unit, an impulse UWB transmitter, and a digital baseband controller. In this paper only the front-end of the module including of the power converter, the RF receiver, the clock generator unit and the impulse UWB transmitter are described.

A. Power Converter

Power converter consists of a chain of 9 stages CMOS voltage multiplier. Figure 5 shows the schematic of the power converter. Except voltage limiter, low threshold voltage MOS is used for all transistors to increase the power efficiency. Normal MOS is used for limiter, in order to decrease the leakage current, which discharges the storage capacitor. During the harvesting time most parts of the module except voltage sensor are off, and the power consumption is very low (less than 1uA). This reduces the real part of the IC's input impedance, hence increases the quality factor, and places high demands on the antenna, which needs to be matched to the IC's input impedance for sufficiently good power efficiency. There are many trades-off between design parameters. Optimization parameters include the number of stages, size of the CMOS transistors, and coupling capacitors. Size of the off-chip storage capacitor depends on the power consumption and operation time of the module. More power consumption bigger storage capacitor, hence longer time is needed to charge it.

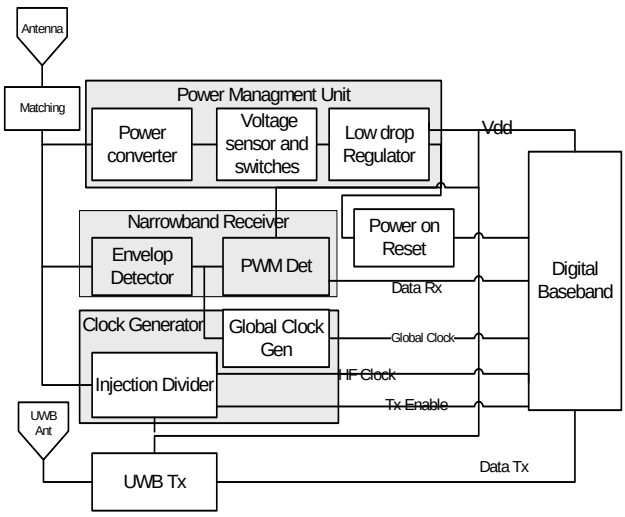


Figure 4. Block Diagram of the Module

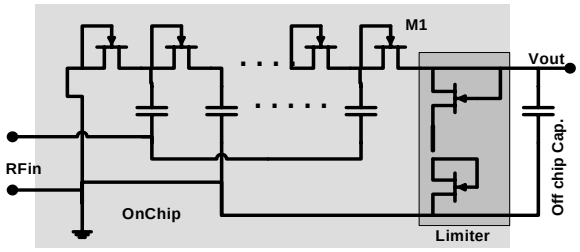


Figure 5. Power converter schematic

B. *Narrowband RF Receiver*

Such as conventional RFID, for downlink from the reader to the tag, RF signal transmitter by the reader is used. The ISM 900 MHz band is chosen for this module. Amplitude shift keying (ASK) modulation and pulse interval encoding (PIE) is utilized. The gaps between pulses (1.5us and 4.5us represent 0 and 1 respectively [7]) are short enough to allow continues power supply of the transponder, but long enough to comply with the stringent bandwidth regulations. Figure 6 shows the downlink RF receiver schematic. It includes an envelope detector and a discriminator circuit which extract data and clock from the received signal. The envelop detector uses the same CMOS voltage multiplier topology than power converter, but with smaller capacitors and only few stages (4 stages). The discriminator circuit decides whether a pulse is long or short and extracts data and clock. Extracted clock is used as the global clock for the baseband control.

C. *Clock Generator*

UWB transmitter requires high frequency clock with low skew and jitter. LC oscillators occupy large area and consume high power. On the other hand, ring oscillator show large variation across the process, temperature and voltage as well as huge phase noise [8]. Utilizing the PLLs which are used in communication systems are not applicable in RFID tag because of their high complexity and power consumption. In this work a low power harmonic injection locked (HIL) divide-by-3 is used to down convert the 900MHz carrier frequency [9]. Figure 7.a shows the schematic of the divide-by-3 circuit.

D. *Impulse UWB Transmitter*

Figure 7.b shows the schematic of the proposed UWB transmitter circuit. It consists of a delay line, a NOR gate and a pulse shaping circuit. The original clock and delayed version of it are applied to the NOR gate. It generates a pulse in every falling edge of the incoming clock. Duration and amplitude of the output pulses are tunable by two control inputs. These controls enable the module to compensate the process and temperature variations, interconnection and packaging effects, as well as the frequency response of the antenna. On the other hand, this ability allows the module to control the output power and bandwidth in different pulse repetition rates and different data rates. In short range applications, when more power is available, high repetition rate pulses transfer data in high speed. On the contrary, to transmit data in longer distance, low repetition rate and high amplitude pulses are chosen. In both cases, amplitude and duration controls enable the module to transmit a signal comply the FCC regulation. On the other hand, the module can balance the power consumption in different pulse repetition rate and data rates by using of these two controls. [10]

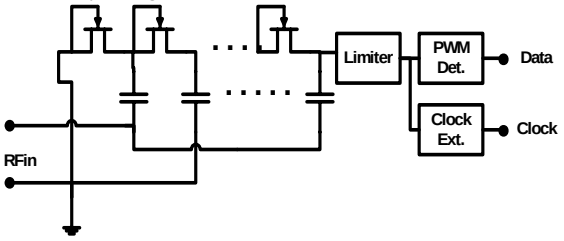


Figure 6. Schematic of Narrowband RF receiver

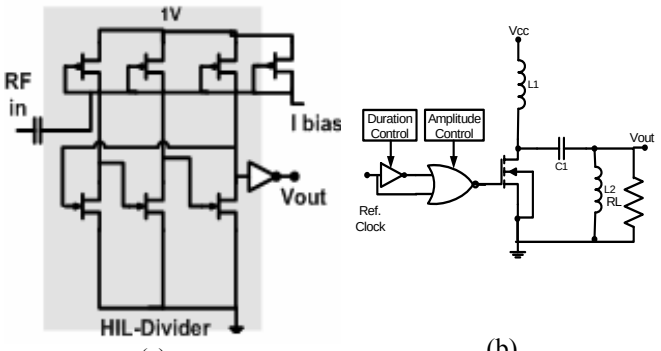


Figure 7. Schematic of a) Clock generator b) UWB transmitter

IV. Results and Discussion

Simulation and analysis results approve the proposed system architecture. At 900 MHz RF signal with -16.2 dBm power, the power converter can provide 2.5V and 1µA output current. It corresponds to 10 meters operation range when 4W EIRP emission is allowed. It is great improvement in operation distance compared with normal RFID which is less than 2m [3]. According to the total power of the module a 200nF capacitor can provide operation current. It takes 580ms time to charge this capacitor with -16.2 dBm input power. If the tag can be identified without any collision, with this charging time reading cycle is at least once per second which is enough for many applications such as tracking, positioning and identification.

Simulation results of the envelope detector and pulse interval encoder show the maximum power consumption of 694nA at 80Kbps data rate. This is a big advantage for self-powered modules, when the operation range is strongly related to the power consumption. Figure 8 shows the simulation results during sending 2 bits of one and zero. The output of envelop detector is used as the global clock in the baseband controller and data is sampled in every falling edge.

Simulation result of the harmonic injection locked divider shows total power consumption of 15.3µA. The minimum input voltage for locking is 100mv which is acceptable for this operation range. Figure 9 shows the output frequency spectrum before and after locking. The Phase noise of the output at 10Hz offset is -85dBc/Hz and jitter is 1.47ps.

Figure 10 shows the output voltage of the UWB transmitter and radiated power spectral density at 100 MHz pulse repetition rate at PPM modulation. Simulation results show the maximum power consumption of 254µA at 100MHz pulse repetition rate and the standby power consumption of 100nA. The results prove that the low data rate UWB communication can be a promising solution for low power applications such RFIDs and wireless sensor networks.

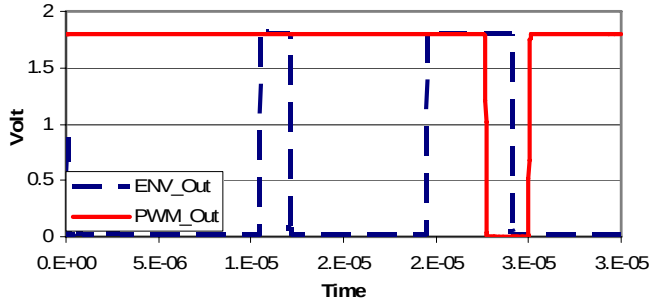


Figure 8. Simulation result of narrowband Receiver

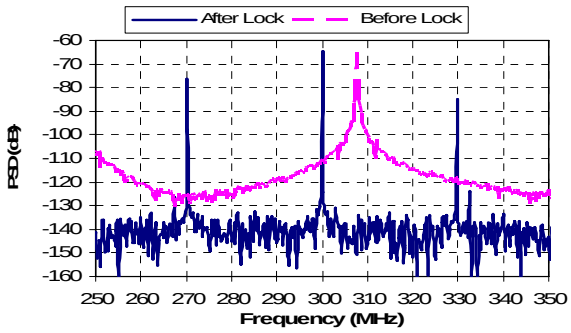


Figure 9. Frequency spectrum of the HIL divider

V. CONCLUSIONS AND FUTURE WORKS

Ubiquitous system based on passive RFID demands for low power and low cost circuit implementation, as well as sufficient tolerant to multi-path fading, and multi-user interference. In this paper, we present a self-powered CMOS radio module with asymmetric wireless links for RFID and ubiquitous sensing. The design is based on CMOS 0.18um process. Such as conventional RFID, it derives the power supply and receives data from the received RF signal. An on-chip power converter charges the off-chip storage capacitor up to 2.5V, with minimum -16.2dBm input power. It corresponds to 10 meters operation range when 4W EIRP emission is allowed.

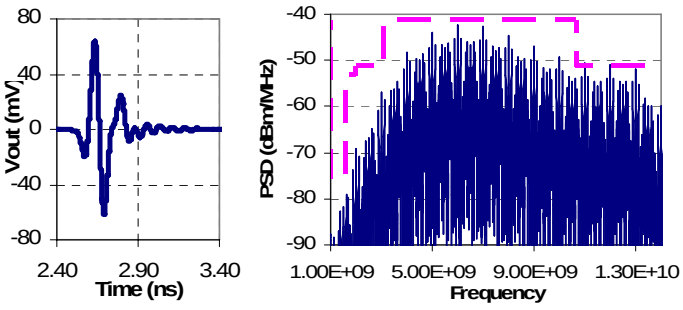
To generate the high frequency clock needed for UWB transmitter a harmonic injection-locked divider is designed. It can lock with minimum input signal of 100mV, while the total power consumption is less than 15.3μA.

A CMOS I-UWB transmitter is utilized in uplink. It consumes maximum 254μA. The output amplitude and duration are tunable which allows the module to transmit a signal meeting the FCC mask in different pulse repetition rates for long and short range applications. This ability could be also used to compensate the process and temperature variations as well as the parasitic effects of packaging and antenna.

Table 1 summarizes the simulation results for the whole module including the baseband and compares the results with some other published works in terms of data rate and power consumption. As can be seen the new module supports higher data rate while consumes much less power compared with others.

A new communication protocol is proposed for the novel system with asymmetric wireless links. It is based on Frame Slotted ALOHA anti-collision algorithm. Dynamic frame size allocation and idle slot skipping methods are investigated and the performance simulation results show a throughput more than 2000 tags per second for the system.

Future work has been oriented by system integration, chip measurement and the reader development.



(a) (b)

Figure 10. UWB Output pulse (a) and its power spectral density (b) (PPM Modulation)

TABLE I RESULTS COMPARISON TO SOME PUBLISHED WORKS.

	[13]	[12]	[11]	This work
Technology	0.13μm	NA	0.35 μm	0.18 μm
Power supply	Battery	Battery	Battery	No battery
TX Freq	1.9GHz	1.9GHz	UWB	UWB
Rx Freq	1.9GHz	1.9GHz	UWB	900MHz
Tx Bit rate	20Kbps	5Kbps	NA	1-10Mbps
Rx Bit rate	20Kbps	5Kbps	NA	40~160Kbps
Tx power consumption	1.45mW	1mW	20mW	496uW
Rx power consumption	3.6mW	450uW	130mW	13.2uW

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