HARTLEY TRANSFORM BASED ARCHITECTURE FOR TIME-FREQUENCY ANALYSIS AND TIME-VARYING FILTERING

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ABSTRACT

An architecture for real-time implementation of a system for time-frequency (TF) signal analysis and time-varying ¯ltering is proposed. It is based on the S-method (SM) and its relationship with the Hartley transform (HT). Hardware design, for a ¯xed-point arithmetic, is well-structured and suitable for VLSI implementation. It is simpler than the system based on the short-time Fourier transform (STFT).

1 INTRODUCTION

Realizations of signal processing algorithms, including TF analysis, admit both hardware and software implementation. Design of an e±cient hardware implementation is often necessary for real-time applications of developed algorithms. Hardware implementations of the simplest tools for TF analysis, the STFT and its energetic version - spectrogram, are widely known. However, a serious drawback of these transformations is low concentration in TF plane, which may be inconvenient in many applications. The quadratic time-frequency distributions (TFDs) play central role in overcoming this problem [7]. The most prominent member of this class of TFDs is the Wigner distribution (WD). Despite the high resolution, it generates cross-terms in the case of multicomponent signals, what limits its applicability. In order to reduce the emphasized e®ects of interference, the reduced interference TFDs are de¯ned [7]. One of them is the SM, which is based on the uni¯ed de¯nition of the STFT and the WD [17]. Recently, the SM has been intensively used [8, 15]. Besides the reduction (or complete elimination) of the cross-terms, the SM retains high resolution of the WD. A hardware implementation of the SM is proposed in [14]. It is based on the STFT implementation. Each channel of the proposed implementation is made of two sub-channels, one for the real part, and the other for the imaginary part of the STFT transformation.

In this paper we develop an architecture suitable for VLSI implementation of the SM based on the HT. The HT is real transform and, for a real-valued signals implementation, it can be more appropriate tool than the STFT. Proposed architecture is then used for the real-time time-varying ¯lter realization. A complete hardware for the e±cient ASIC implementation of a system for TF analysis and time-varying ¯ltering has been presented.

2 THEORETICAL BACKGROUND

A discrete form of the SM is given by [17, 20]:

$$SM(n;k) = \sum_{i=-L_d}^{L_d} P(i)STFT(n;k+i)STFT^*(n;k-i); \quad (1)$$

where STFT of the analyzed signal $f(n)$ is de¯ned as:

$$STFT(n;k) = \sum_{i=-N/2+1}^{N/2} f(n+i)w(i)e^{-j\frac{2\pi}{N}ik}; \quad (2)$$

and $W_P = 2L_d + 1$ is a width of the frequency domain window $P(i)$. By an appropriate selection of the window $P(i)$ width, the same concentration as in the WD case can be achieved, avoiding the presence of cross-terms [17, 20]. Knowing that the STFT of the real analyzed signals is a complex transform, $STFT(n;k) = STFT_{Re}(n;k) + jSTFT_{Im}(n;k)$ ($STFT_{Re}(n;k)$ and $STFT_{Im}(n;k)$ are the real and imaginary part of $STFT(n;k)$, respectively), in the case of rectangular window $P(i)$, (1) can be written as:

$$SM(n;k) = |STFT(n;k)|^2$$
$$+2\sum_{i=1}^{L_d} STFT_{Re}(n;k+i)STFT_{Re}(n;k-i)$$
$$+2\sum_{i=1}^{L_d} STFT_{Im}(n;k+i)STFT_{Im}(n;k-i): \quad (3)$$

Thus, each channel of the SM implementation based on the STFT consists of two identical sub-channels, one used for processing of $STFT_{Re}(n;k)$, and the other used for processing of $STFT_{Im}(n;k)$ [14].

3 HARDWARE FOR THE S-METHOD IMPLEMENTATION BASED ON THE HT

When a signal is real-valued then one may use the HT instead of the STFT, since the HT gives the real coefficients of the real analyzed signal. A discrete form of the short-time HT is given by, [6, 10, 12]:

$$HT(n;k) = \sum_{i=-N/2+1}^{N/2} f(n+i)w(i)(\cos\frac{2\pi}{N}ik + \sin\frac{2\pi}{N}ik): \quad (4)$$

The relation between $STFT(n;k)$ and $HT(n;k)$ is:

$$HT(n;k) = H_p(n;k) + H_n(n;k)$$

$$= STFT_{Re}(n;k) + STFT_{Im}(n;k); \quad (5)$$

where:

$$H_p(n;k) = [HT(n;k) + HT(n;-k)]/2;$$

$$H_n(n;k) = [HT(n;k) - HT(n;-k)]/2: \quad (6)$$

Here, the HT hardware implementation will be based on a recursive algorithm, which can be easily derived in the case of a rectangular window $w(i)$, and represented as:

$$HT(n;k) = F(n)(-1)^k + c(k)HT(n-1;k)$$

$$+s(k)HT(n-1;-k); \quad (7)$$

where $HT(n;-k) = HT(n;N-k)$, $c(k) = \cos(2\pi k/N)$; $s(k) = \sin(2\pi k/N)$, and $F(n) = f(n+N/2) - f(n-N/2)$. It is more suitable for VLSI implementation than the corresponding ones based on (4), since it reduces hardware complexity, [11]. For any other window $w(i)$ type, the HT should be modified in the same manner as the STFT [14, 21]. Based on (3) and (5)-(6), the SM can be written in terms of the HT,

$$SM(n;k) = [HT^2(n;k) + HT^2(n;-k)]/2$$

$$+\sum_{i=1}^{b_d} P(i)[HT(n;k+i)HT(n;k-i)$$

$$+HT(n;-k+i)HT(n;-k-i)]: \quad (8)$$

Note that we can split $SM(n;k)$ into two parts, $SM(n;k) = [SM_+(n;k) + SM_-(n;k)]/2$, where:

$$SM_+(n;k) = HT^2(n;k)$$

$$+2\sum_{i=1}^{b_d} P(i)HT(n;k+i)HT(n;k-i); \quad (9)$$

$$SM_-(n;k) = HT^2(n;-k)$$

$$+2\sum_{i=1}^{b_d} P(i)HT(n;-k+i)HT(n;-k-i): \quad (10)$$

The total number of	I	II
Adders	$2(L_d+2)$	L_d+4
Multipliers	$2(L_d+3)$	L_d+3

Table 1: The total number of adders and multipliers in the SM hardware implementation: I - the SM implementation based on STFT, and II - the SM implementation based on HT

Knowing that $HT(n;-k) = HT(n;N-k)$, follows $SM_-(n;k) = SM_+(n;N-k)$, and consequently,

$$SM(n;k) = \frac{SM_+(n;k) + SM_+(n;N-k)}{2}: \quad (11)$$

The hardware necessary for one channel implementation of the SM with the signal independent window $P(i)$ width, and $L_d = 2$ is presented in Fig.1, blocks 1-2. It has been designed for a 16 bit fixed-point arithmetic. The SM implementation based on the HT (block 2 in Fig.1) needs only a half of the hardware used in the SM realization based on the STFT, [14], since the HT is always real, and $SM_-(n;k) = SM_+(n;N-k)$ (i.e., $SM_-(n;k)$ may be obtained from the $(N-k)$-th channel). It is important to note that the HT realization (block 1 in Fig.1) is simpler than the STFT realization, since the STFT realization includes the realization of its real and imaginary part separately, [14]. The $SM(n;k)$ value is an average of $SM_+(n;k)$ and $SM_+(n;N-k)$, (11). It is realized by a one bit shift to the right. The total number of multipliers and the total number of adders is considerably smaller than it is necessary for real-time implementation based on the STFT, Table 1. The multiplication operation results in two sign-bit and, assuming Q15 format (15 fractional bit), the product must be shifted left by one bit to obtain correct results. This shifter is included as a part of multiplier. The throughput of the system is N. The longest path is one that connects the register storing $HT(n-1;k \S L_d)$, through 2 multipliers and L_d+3 adders, with the output $SM(n;k)$. This path determines the fastest sampling rate. Observe that the SM implementation introduces only an additional delay of L_d adders, compared to the spectrogram implementation. Thus, the fastest sampling rate is essentially the same for both implementations.

Note that the hardware implementation of the signal-dependent SM based on HT can be realized by producing signals which will control the summation in $SM_+(n;k)$ and $SM_-(n;k)$. These signals should stop the summation outside the auto-therm width, defined by the spectrogram, $SPEC(n;k) = \frac{1}{2}[HT^2(n;k) + HT^2(n;N-k)]$, [21].

4 HARDWARE IMPLEMENTATION OF THE TIME-VARYING FILTER

Time-varying filtering is one of the challenging areas where one can benefit from the TFDs. Time-varying

filtering of a nonstationary noisy signal $x(n) = f(n) + \varepsilon(n)$; based on the WD, can be defined, in discrete-time domain, as [5, 13, 16, 18]:

$$(Hx)(n) = \sum_{k=-N/2+1}^{N/2} L_H(n;k) HT_x(n;k); \qquad (12)$$

where $L_H(n;k) = E\{WD_{fx}(n;k)\}/E\{WD_{xx}(n;k)\}$ is the filters' region of support [13, 16, 18]. Note that subscripts are introduced in order to denote the TFDs of signal $x(t)$ at the filter's input, the TFDs of the filtered signal $f(t)$, or their cross-TFDs. Starting from the properties of the SM, and its simple hardware realization, it can be concluded that the introduction of $SM(n;k)$ in $L_H(n;k)$ definition, in the case of multicomponent signal $f(n)$, is an appropriate approximate of $E\{WD(n;k)\}$, when only one noisy signal realization is known [18]. Thus,

$$L_H(n;k) = \frac{SM_{fx}(n;k)}{SM_{xx}(n;k)}. \qquad (13)$$

Besides, the SM implementation includes, as a key intermediate step, the HT realization, which is included in the time-varying filtering definition (12), as well. Thus, the HT realization is used in both: the $L_H(n;k)$ determination and the filter implementation, Fig.1.

Consider a wide class of FM signals $f(n)$, highly concentrated in TF plane (in a tiny region D of the TF plane), corrupted with a white noise $\varepsilon(n)$, widely spread in the TF plane. Now, in the hardware realization of the $k-th$ channel, $L_H(n;k)$ can be determined by comparing the SM value with the spectral floor R [19]. In that way we produce the control signals c_k, as:

$$c_k = \begin{cases} 1; & \text{for } SM_{xx}(n;k) \geq R \\ 0; & \text{for } SM_{xx}(n;k) < R; \end{cases} \qquad (14)$$

that determine which component of $HT(n;k)$ will be forwarded to the output. With a control signal $c_k = 1$, all components $HT(n;k)$, $k = 0;1;:::N-1$, are summed mutually. For a small values of R, filters' region of support tends to the region D, whereas for greater values of R, filters' region of support tends to the instantaneous frequency of the analyzed signal. In the first case, the distortion in the original signal would be overcame, while in the other case the maximal reduction of the noise influence to the filtered signals is performed. Block scheme of the time-varying filter hardware realization is presented in Fig.1.a), while the complete hardware for the time-varying filter implementation is presented in Fig.1.b) (blocks 1-3). The additions may be performed by adding the adjacent components in the first step, then the adjacent sums in the next step, and so on. That scheme corresponds to the butterflies in the FFT algorithms. Namely, each component $HT(n;k)$, $k = 0;1;:::N-1$, with a control signal $c_k = 1$, passes through $\log_2 N$ adders to the output of the system.

Here, we will not present numerical illustration.. For the examples we refer the readers to the papers where the theoretical approach for the methods used in this paper is given, [8, 14, 15, 18, 20]. Also, more details on appropriate register length design are presented in [9].

5 CONCLUSION

An HT based system for TF analysis is proposed. It has considerably simpler hardware implementation than the system based on the STFT. A slight extension in hardware has been proposed for the time-varying filter realization.

6 ACKNOWLEDGMENT

This work is supported by the Volkswagen Stiftung, Federal Republic of Germany.

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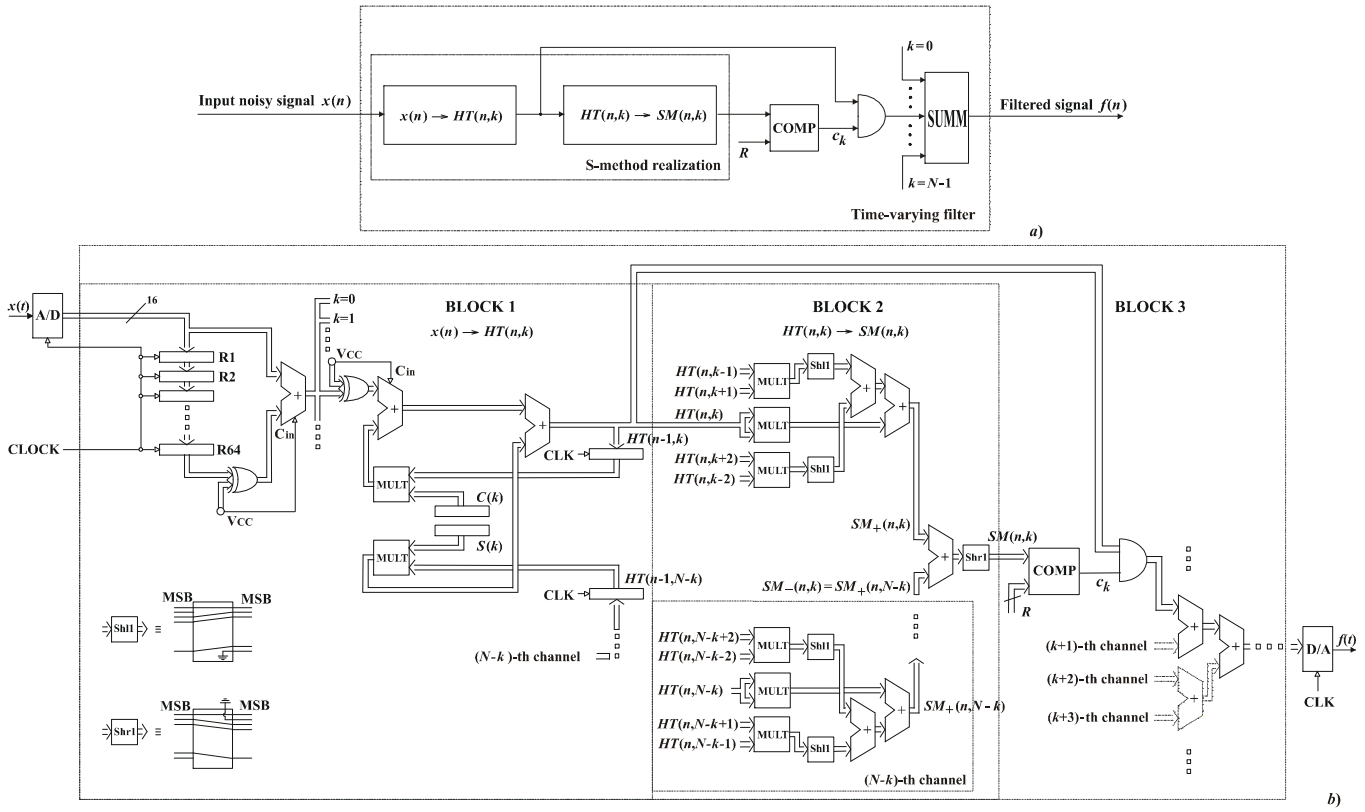

Figure 1: An arcitecture for hardware realization of a system for time-frequency analysis (blocks 1-2) and time-varying ¯ltering (blocks 1-3): a) Block scheme, b) Hardware

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