MULTIPLIERLESS IMPLEMENTATION OF ALL-POLE DIGITAL FILTERS USING A LOW-SENSITIVITY STRUCTURE

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ABSTRACT

Multiplierless filters are natural extensions of the low-sensitivity structures. Some low-sensitivity structures are associated with structural alteration and the resulting multiplier coefficients are different than the initial designed values in these structures. For the cases when coefficient values are quite small, they can be implemented in a multiplierless manner, i.e., by using only few bit shifts and adds and/or subtracts, by converting them to minimum signed powers-of-two (MNSPT) or canonic signed digit (CSD) forms, and the number of nonzero bits required for coefficient representations are quite low. This paper investigates a low-sensitivity unconventional structure that is very suitable for implementing all-pole digital filters. Further, accepting a marginal deviation from the given specifications, the required number of nonzero bits becomes very low, making the overall implementation attractive. Also, one can start with a filter with marginally stricter specifications without increasing the filter order. Then, the modified coefficient values are quantized such that the given overall criteria are still met.

1 INTRODUCTION

Minimum number of signed powers-of-two (MNSPT) or canonic signed digits (CSD) representations of binary digits are extensively used for representing the multiplier coefficients in a multiplierless implementation of a digital filter. An MNSPT representation of a coefficient value is given by $\sum_i a_i 2^{-t_i}$, where each a_i is either 1 or –1 and t_i is a positive or negative integer. For instance, 1.93359375 can be realised as $2–2^{–4}–2^{–8}$. In this example case, the multiplication is more efficiently and economically achieved with aid of three bit shifts and two subtracts than by use of a nine-bit multiplier.

Methods of optimization is one of the major approaches for multiplierless implementations [5–7, 15, 16]. Filter design being basically a problem of approximation due to the tolerances in specifications, optimization methods are used to find the optimal transfer functions under given constraints. It comprises of optimizing the filter coefficient values such that the resulting filter meets the given criteria with its coefficients values being expressible in MNSPT forms. While optimization methods are considered to be quite satisfactory in general, one may not assure or guarantee that the optimal solution will always be found under the given constraints. The solution can be unsatisfactory, for example, in terms of the filter order, the given wordlength of the multipliers, or the specified number of shifts and adds (in the case of multiplierless implementation), or some combination of them. Under such conditions, some parameters or characteristics of the filter have to be relaxed to obtain an acceptable design.

The structures such as sum of allpass filters, including lattice wave digital (LWD) filters, coupled with optimization methods have shown to yield good results for multiplierless implementations [8–11, 15, 16] in the case of IIR filters. These filters are characterized by the attractive property that there exist LWD structures with the number of required multipliers being equal to the filter order, thereby decreasing the number of multipliers compared to conventional realizations.

Another interesting approach is the one that stems from design of an odd-order elliptic minimal Q-factor analog filter (EMQF) that has some special properties [8–11]. These filters are transformed to digital filter using the bilinear transformation and the digital filter is implemented as a sum of two allpass filters [8–11]. The design and the implementation may also be associated with a proper expansion of the space of the design parameters such as passband (stopband) tolerances, edges, and the filter order.

Especially, in the case of FIR filters, another approach is based on combining simple sub-filters that can be implemented using only few shifts and adds and/or subtracts. Although quite attractive, to make this approach as a viable one, a large database of such filters will have to be generated and some optimization method will have to be evolved in order to combine some of them to meet the desired specifications.

The feasibility of implementing multiplierless recursive digital filters based on coefficient translation methods in low-sensitivity structures has been demonstrated in [2, 3]. These low-sensitivity structures are based on replacing the unit delay element by a simple structure [1, 4], that is equivalent of shifting the origin of the z-plane that results in modification of the multiplier coefficients those are to be implemented. These modified coefficients when implemented in MNSPT or CSD forms, require a few shifts and adds and/or subtracts for implementation. Allowing a marginally insignificant deviation in the specifications a gross reduction in number of nonzero bits (effectively the number of shifts and adds and/or subtracts required) was seen to be feasible.

We observe that one low-sensitivity structure in [4], while being unconventional, is capable of reducing sensitivity of a second-order section with poles only to an arbitrary level by varying two parameters. This structure becomes a potential candidate for investigating for using in multiplierless implementations of filters. We utilize this low-sensitivity structure for implementing all-pole filters with an equiripple passband behavior [13, 14] in the multiplierless manner and achieve interesting results.

2 THE STRUCTURE FOR IMPLEMENTATION

The second-order structure for implementing an all-pole section consisting of a pole pair is depicted in Fig. 1. Here, k_1 and k_2 are of the form $\sum_i p_i 2^{t_i}$, where p_i is either 1 or -1 and the t_i's are integers. These multipliers can be realized by using few bit shifts and adds and/or subtracts. a_{1m} and a_{2m}, in turn, are the modified multiplier coefficients. Normally, the maximum of three bits for k_1 and two bits for k_2 are sufficient to reduce the sensitivity below that of the majority of other structures [4].

The values of k_1 and k_2 are chosen depending on the radial distance and the angular locations of the pole pair being located at $z = re^{\pm j\theta}$. Consider the following second-order all-pole transfer function:

$$H(z) = 1/(1 + a_1 z^{-1} + a_2 z^{-2}), \qquad (1)$$

where $a_1 = -2r\cos\theta$ and $a_2 = r^2$. The modified coefficients are given by

$$a_{1m} = (2k_1 - a_1 + x)/2 \text{ and } a_{2m} = -(a_1 + x)/2 \text{ for } 0<\theta<\pi/2 \qquad (2)$$

and

$$a_{1m} = (2k_1 - a_1 - x)/2 \text{ and } a_{2m} = (-a_1 + x)/2 \text{ for } \pi/2<\theta<\pi. \qquad (3)$$

Here,

(i) $x = (a_1^2 - 4a_2 + 4k_2)^{1/2}$.

(ii) k_1 is a few bit approximation closest to
$(a_1 - x)/2$ for $0<\theta<\pi/2$, and
$(a_1 + x)/2$ for $\pi/2<\theta<\pi$.

(iii) k_2 is a few bit approximation closest to a_2 with k_2 being chosen before k_1 ensuring that x remains real.

The realization details and the scaling schemes are similar to those described in [4].

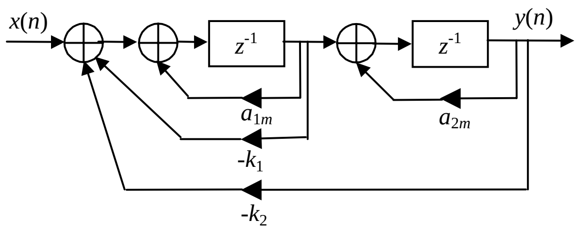

Fig. 1. Modified second-order all-pole section.

3 RESULTS AND DISCUSSIONS

Quite a few all-pole filters were designed according to the very simple design scheme described [13, 14] and were realized with cascaded second-order sections modified in the above-mentioned manner. It was found that for most of the cases one bit each for k_1 and k_2 is sufficient.

The results for some of the filters are shown in Table 1 indicating the number of nonzero bits that would be required for achieving various levels of passband tolerances (the stopband tolerances were generally affected negligibly). For these filters one bit each for k_1 and k_2 was used.

Another filter was designed based on this information, with stricter passband tolerances but without any increase of the filter order. The number of nonzero bits for the revised specification are also shown that gives better passband tolerances than the initial specification and with a much lower number of nonzero bits required for the initial design. To illustrate further, for Filter 1 in Table 1, thirty-eight nonzero bits were required to achieve a 0.5 dB passband variation, whereas for the revised specification only thirty-one nonzero bits are needed to achieve a 0.3 dB passband variation without any increase in the filter order. Similar results are seen for the other filters.

By increasing the number of bits in realizing k_1 and k_2, an overall reduction of one to two shifts and adds and/or subtracts per second-order section is observed in some second-order sections for some filters. Similar reduction was observed when different quantization levels were tried out in different second-order sections for some filters. This fact is expected and natural due to the pole locations (with its associated sensitivity) of the filter.

The proposed scheme can be used for recursive filters with zeros also, with the zeros being implemented separately. Especially, for Chebysev type I filters, the numerator polynomials of the transfer function are of form $(1 + z^{-1})^n$. This numerator polynomial can be implemented by using multiplierless first-order and second-order sections.

The solid and dashed lines in Fig. 2 show, in the case of Filter 1 of Table 1, the amplitude responses for the infinite-precision filter and for the filter obtained using twenty-four nonzero bits (i.e., on the average three nonzero bits per multiplier). It is seen that that the deviation between the infinite-precision and finite-precision designs is very small in the passband. In the transition band and in the stopband the deviation is negligible. Similar results were observed for other filters.

Table 1 The required number of nonzero bits for multiplierless implementations for some filters.

<table>
<tr><th>Characteristics of filters</th><th colspan="2">Details of Realization</th></tr>
<tr><td rowspan="3">Filter 1: 8^{th} order,
passband=0.1π, stopband=0.17π,
passband ripple=0.5 dB,
stopband attenuation= 60 dB

Pole locations:

0.93184802071470 + 0.05833345279549i
0.93184802071470 – 0.05833345279549i
0.92833400083769 + 0.16727232624414i
0.92833400083769 – 0.16727232624414i
0.92739824714529 + 0.25397933648811i
0.92739824714529 – 0.25397933648811i
0.93752236424626 + 0.30625487937977i
0.93752236424626 – 0.30625487937977i</td><td colspan="2">Cascade realization of 2^{nd} order unmodified sections requires 19-bit multipliers</td></tr>
<tr><td>Number of nonzero bits for 8 multipliers</td><td>Passband tolerance obtained</td></tr>
<tr><td>(a) 38

(b) 27

(c) 24

(d) 31</td><td>0.5 dB for filter designed with initial specifications

0.56 dB …….”…….

0.67 dB …….”…….

0.3 dB for filter designed with revised specifications of passband ripple=0.2 dB and stopband attenuation=60 dB</td></tr>
<tr><td rowspan="3">Filter 2: 8^{th} order,
passband=0.15π, stopband=0.285π,
passband ripple=0.05 dB,
stopband attenuation= 60 dB

Pole locations:

0.83870453672116 + 0.08154803312912i
0.83870453672116 – 0.08154803312912i
0.83085909222853 + 0.23628457482504i
0.83085909222853 – 0.23628457482504i
0.82807597938588 + 0.36677551130473i
0.82807597938588 – 0.36677551130473i
0.85015180506249 + 0.45762168906590i
0.85015180506249 – 0.45762168906590i</td><td colspan="2">Cascade realization of 2^{nd} order unmodified sections requires 23-bit multipliers</td></tr>
<tr><td>Number of nonzero bits for 8 multipliers</td><td>Passband tolerance obtained</td></tr>
<tr><td>(a) 46

(b) 37

(c) 31

(d) 33</td><td>0.05 dB for filter designed with initial specifications

0.0535 dB …….”…….

0.0676 dB …….”…….

0.0254 dB for filter designed with revised specifications of passband ripple=0.02 dB and stopband attenuation=60 dB</td></tr>
<tr><td rowspan="3">Filter 3: 8^{th} order,
passband=0.05π, stopband=0.087π,
passband ripple=0.05 dB,
stopband attenuation= 50 dB

Pole locations:

0.94358159369431 + 0.03083842399663i
0.94358159369431 – 0.03083842399663i
0.94822332550403 + 0.08851492817644i
0.94822332550403 – 0.08851492817644i
0.95846996042939 + 0.13447043932229i
0.95846996042939 – 0.13447043932229i
0.97523786211604 + 0.16187943758154i
0.97523786211604 – 0.16187943758154i</td><td colspan="2">Cascade realization of 2^{nd} order unmodified sections requires 25-bit multipliers</td></tr>
<tr><td>Number of nonzero bits for 8 multipliers</td><td>Passband tolerance obtained</td></tr>
<tr><td>(a) 46

(b) 37

(c) 34

(d) 34</td><td>0.05 dB for filter designed with initial specifications

0.057 dB ……”…….

0.079 dB ……”…….

0.0235 dB for filter designed with revised specifications of passband ripple=0.02 dB and stopband attenuation=50 dB</td></tr>
</table>

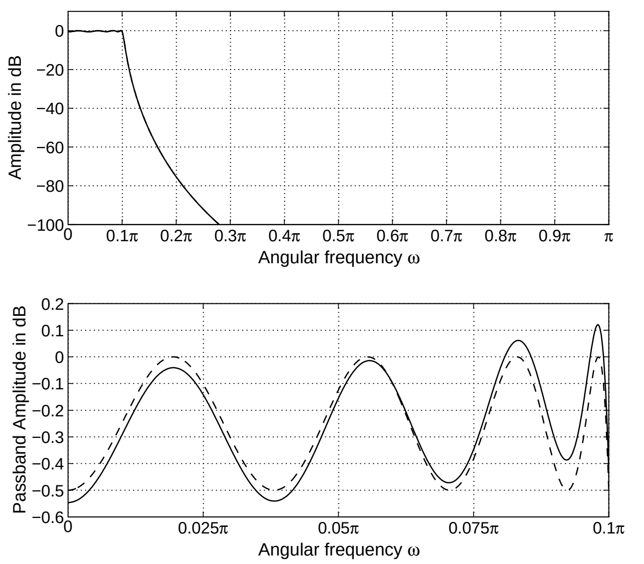

Fig. 2. Amplitude responses in the case of Filter 1 in Table 1 for the infinite-precision filter (dashed line) and for the filter with twenty-four nonzero bits (solid line).

4 CONCLUSIONS

We have shown that the multiplierless implementation of all-pole filter utilizing a typical low-sensitivity structure is a feasible and attractive proposition. Further, considering the acceptance of marginally small deviations in passband and stopband tolerance specifications compared with the initial infinite-precision design, the method becomes quite attractive for implementing all-pole filters in the multiplierless manner. Alternatively, one can start with a design with stricter specification without any increase in the order of the filter. Our analysis indicates that utilizing the approach outlined earlier it is possible to achieve a multiplierless realization with around four nonzero bits per multiplier. Future work is devoted to applying optimization techniques to further reducing the number of nonzero bits.

5 ACKNOWLEDGEMENT

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