A PRML Equalizer for Hard Disk Drives with Low Sensitivity to Sampling Phase Variation

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ABSTRACT

This work presents a new architecture for the realization of Hard Disk Drive Read Channels, using EPR-IV equalization. The pre-equalization is realized as a sampled-data system in order to have precise pulse shaping and simply tunable bandwidth. The equalization is then completed by a fractionally spaced equalizer, which ensures low sensitivity to sampling phase variation. The system complexity is reduced with respect to typical solutions, while the performances are within the usual specs in every operating condition, as confirmed by careful simulations. The architecture was designed to be integrated in a standard CMOS IC.

1 INTRODUCTION

The design of Hard Disk (HD) drive write and read channels, as well as of all the other blocks in a HD system, poses several interesting research challenges. Indeed the constant request for higher data rates and storage densities has resulted in the application of advanced techniques of equalization and detection. For instance the Partial Response Maximum Likelihood (PRML) [1] equalization became a standard for HD drive systems, in order to achieve high data rates. Initially class four partial response (PRIV) has been preferred, but the technology is now ready to resort to Enhanced Class four PRML (EPRIV), which can handle even higher storage densities [2] [3] [4] [5] [6]. The HD equalizer are usually adaptive in order to compensate for time varying parameters; moreover they are frequency tunable, as the system data rate is changing within different disk tracks, and programmable, in order to compensate for storage density variations.

Many different solutions have been proposed to realize these systems, however some commonly used blocks can be singled out. Usually a pre-equalization is performed in the continuos time domain, using a lowpass-filter with, e.g., seven poles and two zeros; then the adaptive equalization is performed in the analog or digital domain. Finally additional digital processing is applied, performing extra equalization and sequence detection. This equalizer is in fact very sensitive to sampling phase variations [7], therefore a timing feedback loop is necessary to compensate for any clock variation.

This work proposes a different solution for an EPRIV equalizer, based mainly on two changes. The first change consists in the realization of the pre–equalizer as a sampled data system, which is more suitable for frequency tuning and transfer function adaptation or programmability [8] and, in addition, can perform more precise pulse shaping. This change prompts the second one. In fact, since the sampled data solution is oversampled, the following step is to apply Fractionally Spaced Equalization (FSE) [9], which is highly insensitive to sampling phase. Therefore in the proposed system the complexity related to sampling phase control is drastically reduced. Moreover the discrete-time processing has shown to give enough signal equalization, so that the typical digital post-equalization is no more needed. This architecture modification reduces the complexity of the system, as it removes a digital filter (usually of high order) and it substantially lowers the resolution (from 6 to 2 bits) required for the A/D present between the analog and the digital processing blocks.

A description of the sampled data pre-equalization and the explanation of FSE are reported in Section 2. In Section 3 simulation results are presented. Conclusions are drawn in Section 4.

2 PROPOSED ARCHITECTURE FOR AN EPR-IV EQUALIZER

This section describes the architecture we propose to realize the EPR-IV equalizer and the procedure that has been followed to design the system.

The overall system architecture is reported in Fig. 1. The first block drawn is a variable gain amplifier (VGA), which compensates for peak amplitude variation of the input signal. Its gain is adjusted in order to minimize the mean of the output error, which is defined as the difference between the detected output signal a and its estimation $\hat{a}$ given by the three level quantizer. Therefore the VGA algorithm can be expressed as:

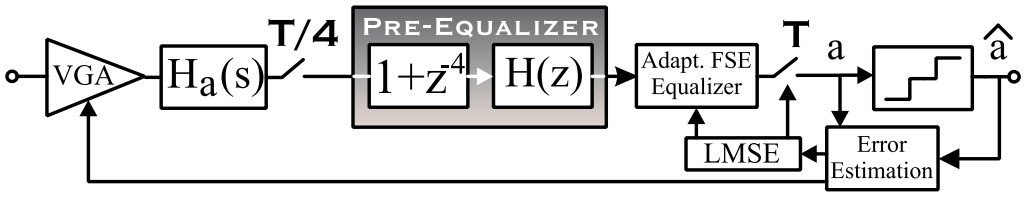

Figure 1: Proposed equalizer architecture

$$\begin{aligned} e_k &= a_k - \hat{a}_k \\ e_{gain}(k) &= |e_k| \cdot |a_k| + |e_{k-1}| \cdot |a_{k-1}| \\ VGA_k &= VGA_k - K_{VGA} \cdot e_{gain}(k) \end{aligned} \quad (1)$$

where k denotes a generic time instant (at T rate), VGA_k is the corresponding VGA gain and K_{VGA} is the step size. It has to be mentioned that at the start of processing the system is driven by a known input, therefore in (1) the error e_k is evaluated using the actual input instead of its estimate $\hat{a}_k$, and a bigger value for K_{VGA} is used.

After the VGA the data path can actually be divided into two main blocks: the first one is devoted to pre-equalize the signal, while the second one implements the actual equalization according to an FSE technique. These blocks are described in the following subsections.

2.1 Sampled Data Pre-Equalizer

To process the signal using a sampled data system a sampling operation must be performed, therefore a continuos time anti-aliasing filter is still necessary. However this block can be non-critical if the system is oversampled: indeed the transition band of the antialiasing filter is increased by the oversampling factor, allowing for low order filters and avoiding problems related to circuit parameters sensitivity. Considering the typical frequency response of HD channels and the system specifications, an oversampling factor of four was chosen in the presented architecture. The antialiasing filter $H_a(s)$ was designed as a a third order Bessel filter.

Once the signal has been sampled, the pre–equalization can be performed in the discrete time domain. It is worthwhile to stress that the signal is now discrete with respect to time only, while its amplitude is continuous, i.e. the signal is still analog. The pre-equalizer was realized as a linear phase FIR filter. Actually, for design purposes, the filter has been ideally divided in two blocks: the first block realizes the transfer function $H(z) = 1 + z^{-4}$ (at the T/4 data rate). This filter ensures that the equalized signal will present a zero at the nominal Nyquist frequency ($f = 1/2T$), which is a typical characteristic of EPRIV. The following FIR filter, $H(z)$, was designed to match the ideal equalization target, which for the EPRIV is given by:

$$H_{EPRIV}(z) = 1 + z^{-1} - z^{-2} - z^{-3} \quad (2)$$

Using this filter a much more precise pulse shaping was achieved, with respect to typical solutions. Indeed the commonly used 7^{th} order filter can only provide some amount of boosting just before the Nyquist frequency, without following any precise equalization target. The proposed approach was a key factor to obtain all the necessary equalization without the need of additional digital post-processing, as shown by the results in Section 3.

In the design of the FIR pre-equalizer one has to trade off circuit complexity for processing precision: indeed, while the filter order must be kept as low as possible to avoid excessive area requirements, it also has to be high enough to correctly approximate the desired frequency response. A six taps FIR filter resulted in the best compromise. The pre-equalizer has also to take care of the fact that the storage density is changing depending on which disk track is being read. Therefore the transfer function of the six taps FIR filter was designed several times, spanning the storage density on the entire range of variation. An appropriate logic will then choose the correct set of taps to be used, while reading a specific disk track. This makes the pre–equalizer programmable.

Usually in standard sampled data systems at this point the signal is downsampled to the nominal data rate and eventually additional processing before detection is performed in the analog or digital domain [8]. However such solution is heavily dependent upon sampling phase, as explained in the next sub-section, which introduces the FSE architecture.

2.2 Fractionally Spaced Equalization

In the frequency response of the HD channel filtered by the FIR filters described above, the signal component beyond the nominal Nyquist frequency ($f = 1/2T$) is not negligible. Therefore if the signal is downsampled to the nominal data rate strong signal degradation due to aliasing will occur. This effect, which is common also in continuos time pre-equalizers, is usually compensated by a timing loop. Indeed the Fourier transform $\tilde{F}(\omega)$ of the resampled signal can be expressed as a function of the Fourier transform of the input signal and the data rate T, according to

$$\tilde{F}(\omega) = \sum_k F(\omega + k\frac{2\pi}{T}) exp[j(\omega + k\frac{2\pi}{T})\tau] \qquad (3)$$

where the dependence from the sampling phase τ is apparent [9]. Therefore the sampling phase has to be be adjusted by the timing loop, in order to have destructive interference within the folded spectrum frequencies, with the clear effect of having a zero at the nominal Nyquist frequency.

This work proposes a different approach, based on Fractionally Spaced Equalization [9]. In this technique the equalization is completely performed at an oversampled data-rate, therefore no aliasing can occur, as the Nyquist frequency is boosted by the oversampling factor. After this processing the signal is downsampled to its nominal data-rate. It is worth to notice that at that point the signal resulting from the downsampling is still dependent on the sampling phase of the first sampler, however to recover the right signal a simple variable delay is enough. The variable delay filtering is usually achieved with an adaptive FIR filter. The FSE was realized using a nine taps transversal adaptive FIR, considering the same tradeoff about the order as for the FIR pre-equalizer. The adaptation is achieved using a Least Mean Squared Error (LMSE) algorithm, in the sign–sign version in order to minimize the hardware requirements. Correspondingly the value of a generic tap c_i at time $k+1$ is given by

$$c_i(k+1) = c_i(k) - K_{step} \cdot |e_k| \cdot |x_i(k)| \qquad (4)$$

where e_k is the error at time k as in (1), $x_i(k)$ is the input sample processed by the tap c_i to produce the output at time k and K_{step} is the step size for the algorithm; as in the VGA case, this parameter has two different values associated with the preamble input (tracking phase) and the effective input (acquisition phase).

Unfortunately this system resulted too sensitive to sampling phase shifts greater than T/4. To overcome this problem a control on the second sampler (T rate) has been introduced. Indeed, varying the phase of this sampler makes it possible to compensate for phase variation by steps of T/4 and therefore makes it possible to revert to the good performance region of the FSE.
Basically when the sampling phase variation exceeds $T/4$, the taps of the adaptive filter, which is trying to compensate such big deviation, manifest a greater variation with respect to the case of small phase shift. Hence such big swing can be detected and the second sampler phase adjusted. The resampler phase is switched only by $T/4$ at once and therefore this re-adaptation process can occur at most three times, since the sampling phase can vary for more than $3T/4$. This fact implies that the convergence time for the adaptive filter can be four times longer than its intrinsic convergence time. A better approach would be to allow the second sampler for larger phase variation, but this case revealed to be more sensitive to instability problem. Since, even in the worst case, the simplest algorithm converges within 100 cycles, which is a usually acceptable period [11], we chose for the more robust implementation. Finally it is worth to notice that the control signal can be extracted directly by the block that controls the adaptive FIR, therefore no additional error extraction is required.

As pointed out in the above description, the order of all the filters present in the system has been kept low enough, in order to realize an area efficient integrated circuit. As the sampling frequency in modern HD channels is approaching 300MHz, the oversampled architecture may become a concern for the bandwidth requirements for Operational Amplifiers. However the Delayed N-Path architectures [10] can easily overcome this problem. Hence all the system requirements are well achievable using switched capacitor circuits in standard CMOS technology [8].

3 SIMULATION RESULTS

The proposed system performances were carefully simulated using MATLAB. It is well established that the HD channel can be modeled as a PAM system, with additive Gaussian white noise [1]. To model the channel impulse response a Lorentian impulse, $l(t)$, can be used, whose analytical expression is

$$l(t) = \frac{1}{1 + (\frac{2 \cdot t}{PW_{50}})^2} \qquad (5)$$

The parameter PW_{50} is the pulse width at half amplitude and is directly related to the disk storage density.

In Fig. 2 the equalizer output is reported for a PW_{50} equal to 2.5 and an input noise corresponding to $SNR =$ 21 dB. Since RLL coding was applied on the written sequence, the EPRIV signal is actually reduced to three output states [2].

As a performance index for the equalizer output, the error probability can be evaluated: for a standard deviation of the noise at the decision point, σ, and a distance d between the threshold values, the probability of error is:

$$P_e = \frac{4}{3} \cdot Q(\frac{d}{2\sigma}). \qquad (6)$$

This quantity has been evaluated for different input noise levels and considering both the best and worst phase shifts. The simulation results are summarized in table below. Comparing these data with the typical results reported in [6], one can conclude that the proposed system performs quite well.

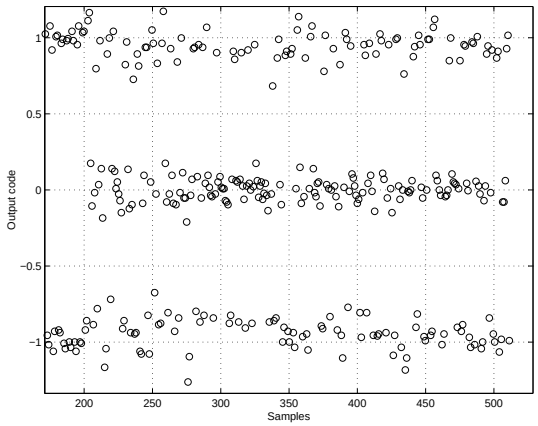

Figure 2: Equalizer output for input SNR=21dB and $PW_{50} = 2.5$

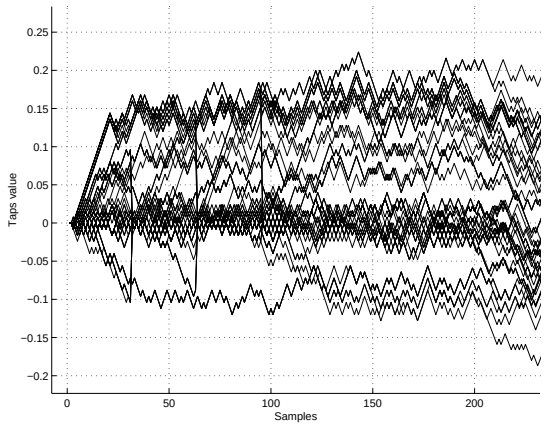

Figure 3: Transient of adaptive filter taps

	P_e	
SNR_{in}	$\tau = 0$	$\tau = 3/4T$
8	$9 \cdot 10^{-6}$	$1 \cdot 10^{-5}$
10	$1 \cdot 10^{-7}$	$2 \cdot 10^{-7}$
13	$2 \cdot 10^{-8}$	$1 \cdot 10^{-8}$
18	$2 \cdot 10^{-9}$	$3 \cdot 10^{-9}$

Finally Fig. 3 shows the transient of the adaptive filter taps corresponding to an input sampling phase greater than $3T/4$. Also in this worst case the convergence time is less than 100 cycles, which is a typical parameter as already mentioned.

4 CONCLUSIONS

In this work an innovative architecture for the realization of EPR-IV read channel for HD drives has been presented. The pre-equalization processing was achieved using a sampled-data architecture. This approach allowed for more precise pulse shaping and for simpler implementation of frequency tuning. The second equalization stage was realized using a fractionally spaced equalizer that is insensitive to sampling phase variations. As a result the proposed architecture does not require a timing loop and a post-equalization in the digital domain. Therefore it has a reduced complexity. As confirmed by simulations the performances of the proposed system are within typical values of conventional solutions in all the possible operating conditions.

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