DEVELOPMENT OF 4 × 4 MIMO-OFDM SYSTEM AND TEST MEASUREMENT

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ABSTRACT

We are developing a compact PCI (cPCI) based prototype of a 4 × 4 multiple-input multiple-output orthogonal frequency division multiplexing (MIMO-OFDM) system for the measurement and analysis of propagation and transmission characteristics in real environments. The target of this system is a MIMO extension of the IEEE802.11a standard, i.e. 5 GHz frequency band, 20 MHz bandwidth. The sampling rates of digital-analog converters (DACs) and analog-digital converters (ADCs) are both 80 Msps, thus enabling 20 MHz bandwidth measurements. In addition, 2 Mgates field programmable gate arrays (FPGAs) are used for pre- and post-processing of each channel, so that we can take advantage of the FPGA's parallel processing capability for simultaneous multichannel processing as well as its reconfigurability for implementation of various MIMO-OFDM algorithms.

1. INTRODUCTION

Improvement of capacity is a major interest for wireless communication systems. In recent years, multiple-input multiple-output (MIMO) systems have attracted a great deal of attention as a promising solution to this issue due to its spectral efficiency[1], and has been studied by many researchers. To investigate the MIMO propagation channel, conventional single-input multiple-output (SIMO) measurement systems, e.g. channel sounders, are extended to deal with MIMO scenarios. These systems enabled measurements including both directions-of-departure (DODs) and directions-of-arrival (DOAs), so-called double-directional channel measurements, which promoted measurement based analyses of MIMO channels.

Previously, we developed a prototype MIMO channel sounder[2] and an instrument based measurement system for MIMO channels[3]. Now we are developing a multipurpose hardware for MIMO systems with reconfigurability like a software defined radio (SDR) by using programmable devices such as field programmable gate arrays (FPGAs). Due to its parallel processing capability, the FPGA is a suitable device for simultaneous multichannel processing for MIMO systems.

Orthogonal frequency division multiplexing (OFDM) is another high data rate transmission technique. Due to its simplicity of implementation and robustness against frequency-selective fading, OFDM is widely used for various applications. One of the applications is the wireless local area network (WLAN). Current WLAN standards such as IEEE802.11a[4], IEEE802.11g[5] and HIPERLAN/2[6] are based on the OFDM technique and have achieved high data rate up to 54 Mbps. For the next generation WLAN systems, MIMO extension of these OFDM based physical layer techniques, i.e. MIMO-OFDM, is the most possible candidate, and new standardization groups such as IEEE 802.11n focus on this technology. From now, it is expected that a variety of MIMO-OFDM algorithms will be proposed, so that we have to compare and evaluate the characteristics of those algorithms with experimental results in real environments. To do that, it is required to implement them on the same platform, where our FPGA based reconfigurable hardware meets the demand. The objective of this paper is implementation of a MIMO-OFDM prototype to verify the operability of MIMO-OFDM systems.

The rest of this paper is organized as follows. In Section 2, we introduce the system overview of our hardware. In Section 3, we briefly describe the model of our target MIMO-OFDM system. Next, in Section 4, a test measurement is demonstrated. Finally, conclusions are drawn in Section 5.

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Table 1: Specifications of hardware.

Center Frequency	5040, 5060, 5080 MHz
RF Local	4470, 4490, 4510 MHz
IF Local	570 MHz
Transmit Power	15 dBm max
DAC	14bit, 80 Msps
ADC	14bit, 80 Msps
Bus Throughput	5.12 Gbps (128bit, 40MHz)

2. HARDWARE

Our developed hardware consists of several compact PCI (cPCI) based component modules such as,

- Digital signal processor (DSP) module
- Digital-analog (D/A) module
- Analog-digital (A/D) module
- Up/down converter module
- Local module

and these modules are assembled to build up a MIMO transceiver. Our MIMO transceiver architecture is drawn in Fig. 1, and some specifications of our hardware are given in Table 1.

2.1 DSP Module

The DSP module is mainly used for controlling the whole system and bit level signal processing for the transmitter and

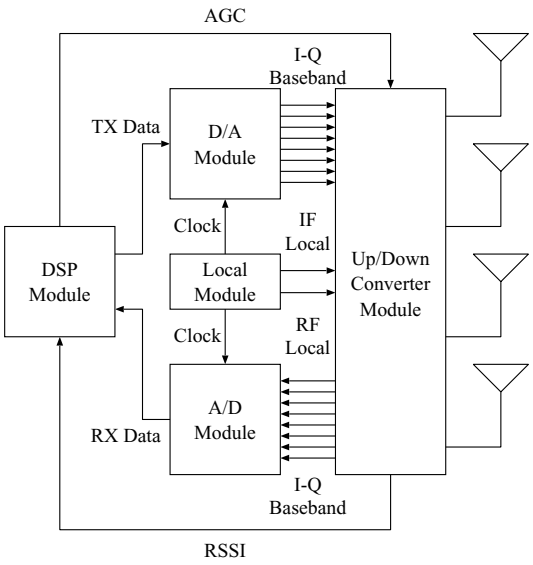

Figure 1: MIMO transceiver architecture.

Figure 2: DSP module.

receiver, e.g. space-time coding and decoding. A photograph of this module is shown in Fig. 2. This module mounts three FPGAs, one for the controller and the others for transmitting (TX) and receiving (RX) data processing. The FPGAs used in our hardware (including D/A and A/D modules) are all 2 Mgates Xilinx Virtex II devices, therefore relatively large scale processing can be implemented. Moreover four parallel DSPs are also embedded for floating point signal processing.

2.2 D/A Module

The D/A module has eight digital-analog converter (DAC) output ports and each pair of ports are connected to an FPGA through a 128k-word FIFO used as a buffer. The FPGA located in the center of Fig. 3 is the controller of this module, which handles data transfer and state control. TX data from the DSP module are fed into this FPGA via the cPCI data bus, and delivered to each channel.

2.3 A/D Module

The A/D module has eight analog-digital converter (ADC) output ports, where the layout of this module (ADCs, FIFOs

Figure 3: D/A module.

Figure 4: A/D module.

and FPGAs) is similar to that of the D/A module (see Fig. 4). Received signals are sampled at the ADCs, pre-processed in each FPGA and gathered at the central FPGA. These data are transferred to the DSP module via the cPCI data bus in the opposite way as the D/A module.

2.4 Up/down Converter Module

The up/down converter module up converts four IQ baseband signals to 5 GHz band radio frequency (RF) signals and vice-versa, where duplex operation is switched automatically through a control signal. Since this module adopts a heterodyne architecture, both up conversion and down conversion are performed through an intermediate frequency (IF) of 570 MHz. In addition, received signal strength indicators (RSSIs) are available for TX/RX control such as automatic gain control (AGC) and carrier sense.

2.5 Local Module

The local module provides 80 MHz clocks for the D/A and A/D modules as well as IF and RF local oscillators for the up/down converter module. Since DACs and ADCs are driven by these clocks, wideband measurement of 20 MHz bandwidth can be performed. This module is locked to a 10 MHz Rubidium frequency standard.

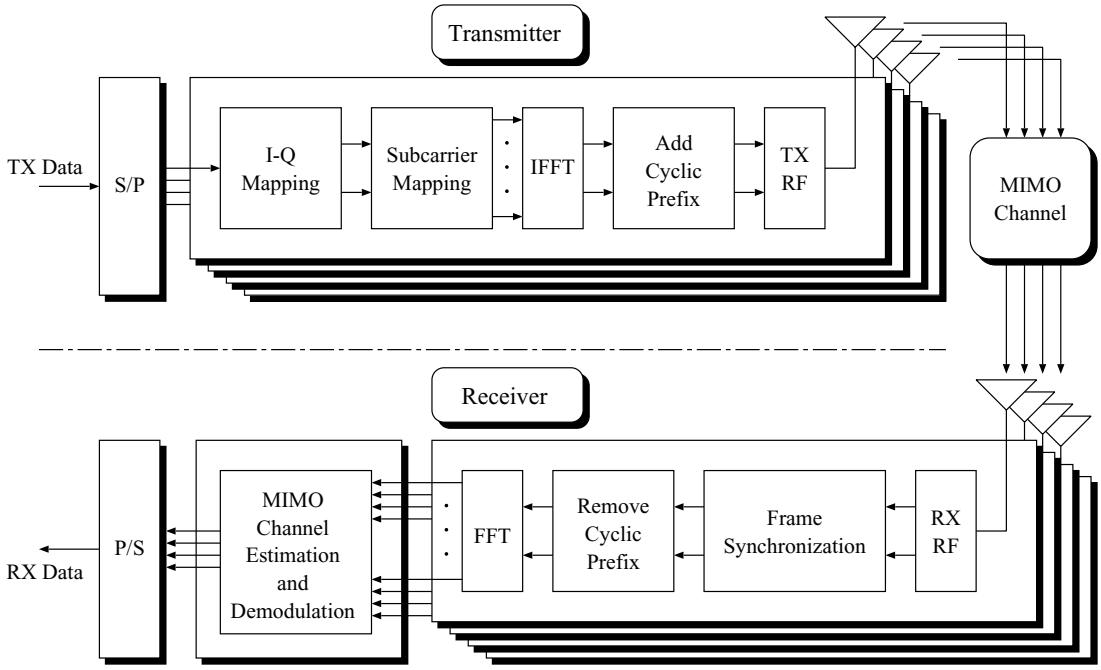

Figure 5: 4 × 4 MIMO-OFDM system model.

3. SYSTEM MODEL

The system model under consideration is depicted in Fig. 5, which shows a MIMO-OFDM system with four TX antennas and four RX antennas. The 4 × 4 MIMO configuration is suitable for our hardware with respect to the number of channels.

The TX data are allocated to four branches. Each branch modulates the data into an OFDM signal and adds a cyclic prefix (CP) as a guard interval (GI). The OFDM signals are then simultaneously transmitted from each antenna and pass through a MIMO channel to the receiver. At the receiver side, preamble detection is the first operation, which is equivalent to rough synchronization in time domain (frame synchronization). Then it is followed by removal of the CP and FFT operation. After that, channel estimation is performed on each subcarrier to obtain the channel matrix **H** used for MIMO demodulation.

The preamble format is given in Fig. 6. Preamble 1 and preamble 2 correspond to the short and long training parts of IEEE802.11a preamble respectively, where preamble 2 is extended for MIMO. Since preamble 1 is the repetition of the same waveform (**t**) ten times, preamble detection is performed by taking the autocorrelation of this part. The length of preamble 2 is extended depending on the number of TX antennas (N_t). **T** in Fig. 6 is the same as the long training symbol of IEEE802.11a, while -**T** is the sign inversion of **T**. This sign pattern is decided according to the N_t-th order Hadamard matrix. Therefore the orthogonality among branches is maintained.

4. TEST MEASUREMENT

As the first step of development, we implemented a ROM based off-line measurement system. At the transmitter side (D/A module), the OFDM waveform data are stored in

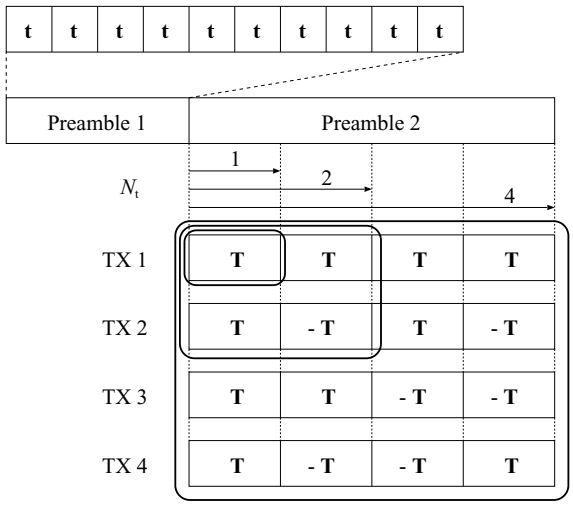

Figure 6: Preamble format.

ROMs inside each FPGA and transmitted repeatedly. Then the receiver (A/D module) samples the RX signals and stores them in ASCII files. The frame synchronization, channel estimation and demodulation are processed in a PC. System parameters are given in Table 2. We applied 4-time oversampling for waveform shaping at the transmitter. Fig. 7 shows the power spectrum of the transmitted waveform data, which is normalized by its maximum value. Due to oversampling, the spectrum fits within the spectrum musk of the IEEE802.11a standard as illustrated by the broken line.

A test measurement was conducted in a typical non line-of-sight (NLOS) office environment. The measured average signal-to-noise ratio (SNR) was 19 dB. Fig. 8 shows the

Table 2: System parameters.

Parameter	Value
Modulation	BPSK
Bandwidth	20 MHz
Number of Subcarriers (Total)	64
Number of Subcarriers (Data)	48
OFDM Symbol Duration	4 μs
Guard Interval	0.8 μs

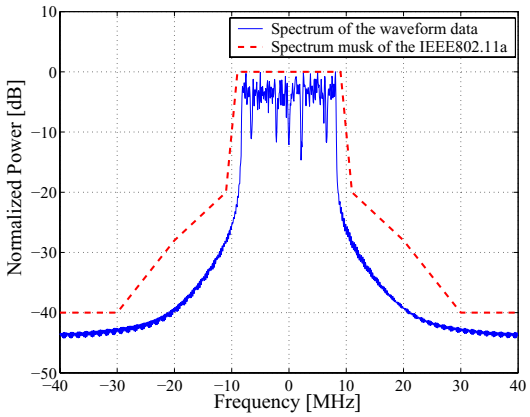

Figure 7: Power spectrum of the transmitted waveform data.

48 data symbols in an OFDM symbol received at a branch, where the frame synchronization, removal of the CP and FFT are already performed. Since the symbols just after FFT are mixed up with those of other branches, the phases of which are rotated as drawn in Fig. 8. Here, we apply the zero-forcing criterion on each subcarrier, i.e.

$$\hat{\mathbf{s}} = \mathbf{H}^{-1}\mathbf{r},$$

where $\mathbf{r}$ is the received signal vector and $\hat{\mathbf{s}}$ is the estimated transmitted signal vector on the same subcarrier of all branches. By doing this, the transmitted symbols are demodulated as shown in Fig. 9. Although we have much to do for improvement, e.g. frequency synchronization and more accurate channel estimation, it seems that we have good prospects for the operability of MIMO-OFDM systems.

5. CONCLUSION

We developed a cPCI based MIMO hardware platform for the measurement and analysis of propagation and transmission characteristics in real environments. The first application of our hardware is a 4 $\times$ 4 MIMO-OFDM system since the MIMO-OFDM technique is a promising solution for the next generation wireless communication systems to achieve higher throughput. In this paper, a test measurement of a MIMO-OFDM prototype is demonstrated and we can find operability on MIMO-OFDM systems. From now, we will implement various MIMO-OFDM algorithms on our reconfigurable hardware, compare the validity of those algorithms and optimize them.

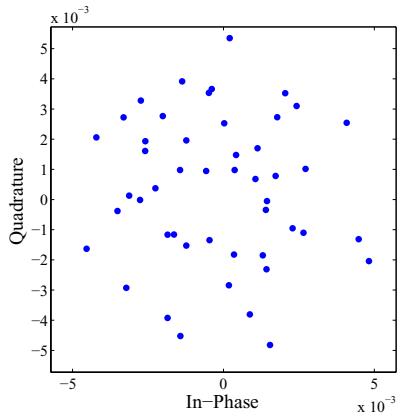

Figure 8: Data symbols before zero-forcing.

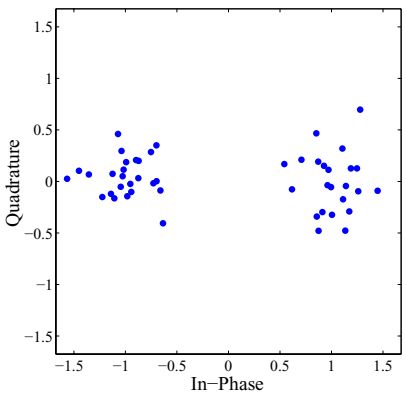

Figure 9: Zero-forcing result.

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