# DIGITAL I&Q DEMODULATION IN ARRAY PROCESSING: THEORY AND IMPLEMENTATION

*David Bernal, Pau Closas, Juan A. Fernández–Rubio*

Dept. of Signal Theory and Communications, Universitat Politècnica de Catalunya (UPC)
Jordi Girona 1-3, Campus Nord, 08034 Barcelona, Spain.
e-mail: {bernal,closas,juan}@gps.tsc.upc.edu
http://gps-tsc.upc.es/comm

## ABSTRACT

Following the IF sampling strategy, a receiver is able to overcome inherent limitations of conventional I&Q demodulators, performing this operation in a completely digital manner. In this paper, IF sampling is analyzed both from theoretical and implementation points of view for the case of an antenna array based receiver. Both analysis are complementary and provide useful guidelines for the design of Software-Defined Radio receivers. The foundations of IF sampling strategy are presented and the design of all-digital I&Q demodulators is covered. Finally, an application to the design of a S-DMB receiver is also presented and FPGA implementation issues discussed.

## 1. INTRODUCTION

In communication systems, a signal is baseband modulated in its in–phase (I) and quadrature (Q) components, which are transmitted to the Radio Frequency (RF) spectrum. Receivers are in charge of demodulating the I&Q components of the received signal. A conventional I&Q demodulator is shown in Figure 1. Basically, it consists in splitting the received signal and multiplying each arm by a local oscillator (LO) and its $90^o$ shifted version. This procedure provides I&Q components after lowpass filtering and quantization. A number of errors may appear when considering the conventional approach shown in Figure 1, mainly caused because the two arms must be closely matched for correct demodulation, e.g. gain balance, quadrature-phase balance or DC offsets. New trends following the Software-Defined Radio (SDR) philosophy emerged [1, 2], mainly thanks to recent advances in high-speed analog-to-digital converters (ADC), that allow IF sampling strategies to be envisaged and the I&Q demodulator to be implemented digitally, overcoming some of the aforementioned errors [3]. Certainly, the analog components of the RF/IF chain have to be still carefully designed. However, a direct downconversion might be unaffordable in high-speed applications [4].

This paper presents both theoretical and implementation aspects of IF sampling, focusing on the demodulation of I&Q components in a completely digital fashion. Section 2 provides a detailed overview of IF sampling strategies and the signal processing involved. Although
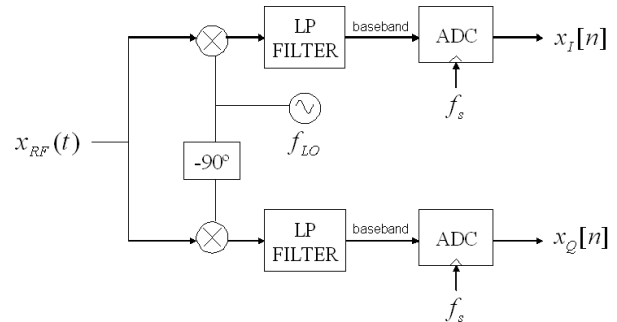
Figure 1: Conventional I&Q demodulator.

this is an increasingly used technique in SDR receivers [5], this paper presents useful design guidelines. In addition, the case of an antenna array receiver is addressed, where the use of Matched Filters may not be possible due to area constraints in the digital platform. The latter introduces a spurious interference, whose impact is discussed from an array processing point of view. Section 3 is devoted to the implementation concerns of digital I&Q demodulation. Finally, Section 4 presents an application to the design of a S-DMB receiver [6] in the S-band. The resulting design has been programmed in VHDL code and implemented in an FPGA device, some results are discussed.

## 2. DIGITAL I&Q DEMODULATION: THEORY

A complex baseband signal $b(t)$, that has a bandwidth of $B$ Hz, is transmitted at RF. We define $b_I(t)$ and $b_Q(t)$ as the in-phase and quadrature components of $b(t)$. After downconversion to an Intermediate Frequency, $f_{IF}$, the signal is bandpass filtered at the receiver to avoid aliasing and to remove high-frequency components. Thus, at the output of the RF chain, the received real signal consists of the desired IF signal corrupted by noise:

$$x_{IF}(t) = a\, V(t) \cos\left(2\pi f_{IF} t + \Theta(t)\right) + \nu(t) \quad (1)$$

where $a$ is the amplitude of the signal and $\nu(t)$ is additive noise. $V(t)$ and $\Theta(t)$ are the envelope and the phase of $b(t) = b_I(t) + j b_Q(t)$, respectively. The IF signal feds an ADC which samples signal at a sampling rate of $f_s = 1/T_s$ with $n_b$ bits of quantization. Hence, the sampled version of the IF signal can be expressed as:

$$x_{IF}[n] = a\, V[n] \cos\left(2\pi f_{IF} n T_s + \Theta[n]\right) + \nu[n] \quad (2)$$

The idea behind digital IF sampling is to undersample IF signal in order to obtain a replica of the signal at baseband, without requiring an additional downconversion. This can be accomplished by properly choosing $f_{IF}$ and $f_s$. In general, the following relations

$$
\begin{aligned}
f_{IF} &= k f_s \pm \frac{f_s}{4} \quad , \forall k \in \mathbb{Z} \mid k \geq 1 \\
f_s &\geq 4B
\end{aligned}
\tag{3}
$$

ensure that a non-overlapped alias will appear centered at $f_s/4$. Then, one of the replicas at $\pm f_s/4$ can be downconverted to baseband using the frequency-shifting property of the Fourier transform of a signal, i.e., $Z(f \pm f_o) \overset{F}{\leftrightarrow} z[n]e^{\mp j2\pi f_o n T_s}$. With $f_o = f_s/4$, it results that we have to multiply the IF signal by $e^{-j\frac{\pi}{2}n}$ to shift the spectrum to the left. Actually, this is a straightforward operation since the sequence of cyclic values of $e^{-j\frac{\pi}{2}n}$ are $\{1, -j, -1, j\}$, where $j^2 = -1$. As shown in Figure 2, this provides the I and Q components of the desired signal.

$x_{IF}[n]e^{-j\frac{\pi}{2}n} = \left[x_{IF}[0], -jx_{IF}[1], -x_{IF}[2], jx_{IF}[3], x_{IF}[4], -jx_{IF}[5], -x_{IF}[6], jx_{IF}[7], \ldots\right]$
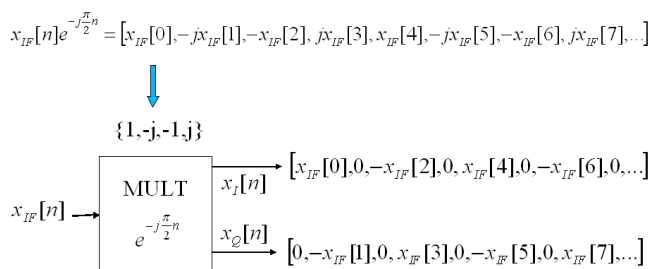


Figure 2: After frequency-shift, I&Q components are obtained.

Figure 3 shows the spectra of the signals involved in the process. $S_{IF}(f)$ is the spectral density of the received IF signal in equation (1). Setting $f_{IF} = 3f_s/4$, i.e. $k = 1$, and sampling $x_{IF}(t)$ according to equation (3), we can observe in Figure 3 that aliasing appears without overlapping in its spectrum $S_{IF}^{adc}(f)$ - recalling that we have assumed a band-limited signal $V[n]$. After frequency-shift, we obtain a baseband replica of the desired signal in $S(f) = S_{IF}^{adc}(f - f_s/4)$.

Notice that the spectral density $S_{IF}^{adc}(f)$ shown in Figure 3 is obtained for any chosen $k$ in (3). Thus, the selection of $k$ is related to implementation issues, i.e., to select a suitable $f_{IF}$ for the application under design. The restriction on $f_s$ to be a minimum of twice the Nyquist frequency arises in order to avoid overlapping in $S_{IF}^{adc}(f)$. After lowpass filtering $S(f)$ one can decimate the signal up to a factor that depends on the chosen sampling frequency.

Now we consider the case of an antenna array based receiver and provide a detailed analysis of the digital signal processing involved in the digital I&Q demodulation procedure. In an $N$ element antenna array, each antenna element receives a different replica of signal in (1), with a different gain and phase depending on the array geometry and the Directions Of Arrival (DOA) [7, 8]. Assuming the narrowband array assumption, consisting of taking the time required for the signal to propagate
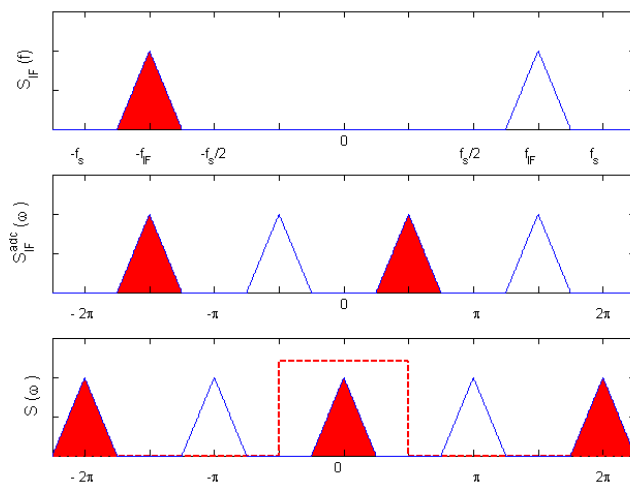


Figure 3: Up-down: spectral densities of $x_{IF}(t)$, $x_{IF}[n]$ and $x[n] = x_{IF}[n] \cdot e^{-j\frac{\pi}{2}n}$.

along the array as much smaller than its inverse bandwidth, a phase shift can be used to describe the propagation from one antenna to another. Hence, it can be assumed that the signal waveform is identical in each element of the antenna array for a given instant. For the $i$–th antenna element, the single snapshot signal model for an arbitrary antenna array geometry is given by

$$
x_{IF}^i[n] = g_i \, a \, V[n] \cos\left(2\pi f_{IF} n T_s + \Theta[n] - \gamma_i\right) + \nu^i[n]
\tag{4}
$$

where $g_i$ and $\gamma_i$ are the gain and phase of the $i$–th antenna element respectively. $\nu^i[n]$ is the additive noise contribution to $x_{IF}^i[n]$. Setting hereafter $f_{IF} = 3f_s/4$ for the sake of clarity, we can express the snapshot model as:

$$
x_{IF}^i[n] = g_i \, a \, V[n] \cos\left(\frac{3\pi}{2}n + \Theta^i[n]\right) + \nu^i[n]
\tag{5}
$$

where $\Theta^i[n] \triangleq \Theta[n] - \gamma_i$. The cosine can be expanded as

$$
\cos\left(\frac{3\pi}{2}n + \Theta^i[n]\right) = \tag{6}
$$
$$
\cos\left(\frac{3\pi}{2}n\right)\cos\left(\Theta^i[n]\right) - \sin\left(\frac{3\pi}{2}n\right)\sin\left(\Theta^i[n]\right),
$$

with the sequences of cyclic values with $n$:

$$
\begin{aligned}
\cos\left(\frac{3\pi}{2}n\right) &= \frac{1}{2}j^n\left(1 + (-1)^n\right) \in \{1, 0, -1, 0\} \tag{7} \\
\sin\left(\frac{3\pi}{2}n\right) &= -\frac{1}{2}j^{n+1}\left(1 - (-1)^n\right) \in \{0, -1, 0, 1\}
\end{aligned}
$$

When multiplying $x_{IF}^i[n]$ by the complex exponential $e^{-j\frac{\pi}{2}n}$ we obtain that the I&Q components of the resulting signal are:

$$
\begin{aligned}
x_I^i[n] &= g_i \frac{a}{2} V[n] \cos\left(\Theta^i[n]\right)(1 + (-1)^n) + \tilde{\nu}_I^i[n] \\
x_Q^i[n] &= g_i \frac{a}{2} V[n] \sin\left(\Theta^i[n]\right)(1 - (-1)^n) + \tilde{\nu}_Q^i[n] \tag{8}
\end{aligned}
$$

being $\tilde{\nu}_I^i[n]$ and $\tilde{\nu}_I^i[n]$ the I&Q components of the resulting noise, $\tilde{\nu}^i[n] = \nu^i[n] \cdot e^{-j\frac{\pi}{2}n}$. Then, the complex baseband signal can be expressed, for each antenna element, as

$$
\begin{aligned}
x^i[n] &= x_I^i[n] + j x_Q^i[n] \qquad\qquad (9)\\
&= g_i \frac{a}{2} V[n] \left[ e^{j\Theta^i[n]} + (-1)^n e^{-j\Theta^i[n]} \right] + \tilde{\nu}^i[n]\\
&= \frac{a}{2} b[n] g_i e^{-j\gamma_i} + \frac{a}{2} b^*[n] (-1)^n g_i e^{j\gamma_i} + \tilde{\nu}^i[n]
\end{aligned}
$$

Arranging signals from elements in row vectors, baseband signal in (9) can be expressed as

$$
\mathbf{x}[n] = \frac{a}{2} b[n] \mathbf{s}_d + \frac{a}{2} b^*[n] (-1)^n \mathbf{s}_d^* + \mathbf{n}[n] \qquad (10)
$$

where

- $\mathbf{x}[n] = \left[ x^1[n], \ldots, x^N[n] \right]^T \in \mathbb{C}^{N\times 1}$ is the signal vector whose rows corresponds to each antenna IF-sampled output.

- $\mathbf{s}_d = \left[ g_1 e^{-j\gamma_1}, \ldots, g_N e^{-j\gamma_N} \right]^T \in \mathbb{C}^{N\times 1}$ is the steering vector of the signal, i.e., a row vector containing the response of the elements to the direction of the signal.

- $\mathbf{n}(t) = \left[ \tilde{\nu}^1[n], \ldots, \tilde{\nu}^N[n] \right]^T \in \mathbb{C}^{N\times 1}$ represents additive noise and all other disturbing terms.

The spectral contribution of the two signal terms in equation (10) can be observed in Figure 3, for the case of a single antenna $\mathbf{s}_d = 1$. The first term corresponds to the desired baseband signal, $b[n]$. The second term, $b^*[n](-1)^n$, corresponds to replicas centered at $\pm f_s/2$, being uncorrelated with $b[n]$. As shown in Figure 3, $x[n]$ can be low-pass filtered with two Matched Filters (I&Q) in order to recover $b[n]$ reducing the contribution of $b^*[n](-1)^n$.

However, when considering an antenna array, it could happen that the use of $2 \cdot N$ Matched Filters in parallel requires an unaffordable computational cost and that matched filtering must be performed at the output of the antenna array, after beamforming. In that case, it is seen from equation (10) that, in addition to the desired signal, an interference is caused by $b^*[n](-1)^n$ being its steering vector the complex conjugate of $\mathbf{s}_d$. Particularizing for the case of a planar array, it is straightforward to observe that the conjugate of $\mathbf{s}_d$ corresponds to the steering vector of the specular multipath of $b(t)$. Thus, if beamforming is performed, the computed weights according to any optimal criteria will attempt to null the direction where the *fictitious* specular replica appears. For the case of a conformal array, it is not apparent that $\mathbf{s}_d^*$ represents an actual steering vector.

## 3. DIGITAL I&Q DEMODULATION: FPGA IMPLEMENTATION

Due to the inherent nature of the parallel processing in an antenna array receiver, it is apparent that an FPGA device is a proper platform. In addition, this platform provides high degrees of reconfigurability, following the SDR philosophy.

Apart from avoiding the above cited inherent errors of conventional approaches, some particularities of an all-digital I&Q demodulator are of interest when addressing its implementation.

Comparing the diagrams of a conventional and an all-digital I&Q demodulator, Figures 1 and 4 respectively, it arises that the number of input pins to the digital platform has been reduced to a half since only the sampled real IF signal is required - considering that the digital platform is located after ADCs in both schemes. Thus, for an $N$ element array where the ADC samples at $f_s$ and quantizes with $n_b$ bits in parallel we would require $N \cdot n_b$ inputs to perform digital I&Q demodulation, instead of the $2 \cdot N \cdot n_b$ delivered in the conventional approach.
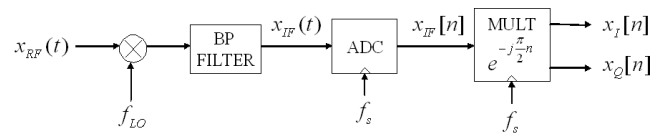


Figure 4: Digital IF sampling with I&Q demodulation.

As could be devised from Figure 2, the implementation of $x_{IF}[n] \cdot e^{j\frac{\pi}{2}n}$ is straightforward in an FPGA. This process only requires to split into two arms even and odd samples and then, multiply each arm with a cyclic sequence of $\pm 1$ values. The latter operation is performed at $f_s/2$, since null-values in-between do not need to be multiplied. The proposed architecture is shown in Figure 5, along with the operating function at each point. Actually, the product by $\pm 1$ does not requires a multiplier, as only the two's complement is performed when multiplying by $-1$ and a bypass for the case of 1, saving computational resources. Additionally, one can decimate each arm in order to remove the null-values. This decimation will reduce the operating frequency of the FPGA to $f_s/2$, since the block in Figure 5 is located immediately after signal has been delivered to the FPGA. This can be performed at the expenses of more laborious designs. This is of interest in high-frequency applications, where FPGAs do not operate efficiently, reducing the operating frequency.
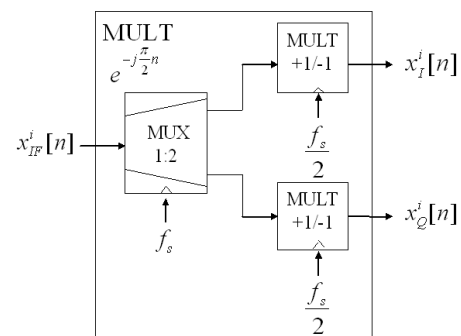


Figure 5: Implementation of the $e^{-j\frac{\pi}{2}n}$ product at the $i$-th array element.

## 4. APPLICATION TO THE S-DMB STANDARD

The general concepts presented along Sections 2 and 3 have been applied to the design of an antenna array based S-DMB receiver under the SDR paradigm for S-band operation. S-DMB is designed to provide satellite and complementary terrestrial on–channel repeater services for high–quality audio and multimedia data for vehicular, portable and fixed reception [6]. The main characteristics of the system are now presented (those which are of interest for the design of the digital I&Q demodulator). A satellite transmits 30 channels multiplexed using CDMA on QPSK modulation at $f_{RF} = 2642.5$ MHz. The chip rate is $r_c = 16.384$ MHz, the processing gain 64 and the transmitted signal is filtered by a square–root raised cosine with a roll-off factor $\rho = 0.22$. Due to acquisition and tracking issues it is desirable to have at least 4 samples per chip, for this reason it has been set $f_s = 4r_c = 65.536$ MHz, $n_b = 8$ bits and, according to equation (3) with $k = 1$, $f_{IF} = 49.152$ MHz. Notice that with this design we ensure the condition in equation (3), $B = (1 + \rho)\frac{r_c}{2} \le 4f_s$.

An antenna array receiver ($N = 40$) has been designed, being the digital platform programmed in VHDL code and synthesized into a Xilinx FPGA device. Beamforming with antenna arrays consists of several antennas, whose outputs are controlled in phase and gain, i.e., multiplied by complex weights, in order to achieve a gain pattern that can be manipulated electronically. Then, all the weighted signals are combined to obtain a single output $y[n]$. These mentioned weights can be stacked in a complex–valued vector $\mathbf{w} \in \mathbb{C}^{N \times 1} = [w_0, \cdots, w_{N-1}]^T$, and the output signal of the beamformer can be computed as $y[n] = \mathbf{w}^H \mathbf{x}[n]$. Weight vector $\mathbf{w}$ can be designed following several criteria, usually exploiting the spatial filtering provided by antenna arrays. Since the aim of the present paper is to study digital I&Q demodulation, we now emphasize on this subsystem of the whole receiver presented in [9]. For the sake of clarity, Figure 6 presents the block diagram of the Digital Beamforming receiver and the location of the digital I&Q demodulation block in it, which consists in a bank of $N$ I&Q demodulators in parallel, similar to that shown in Figure 5. Notice that, for this application, the IF sampling strategy results especially helpful as it reduces the number of signal input pins to the FPGA from 640 to 320, apart from avoiding errors of conventional I&Q demodulators.

The schematic description of the digital I&Q demodulator is shown in Figure 7. Other attempts to implement digital I&Q demodulators can be found in the literature [5, 10, 11, 12] for other communication systems. Nevertheless, the schematic in Figure 7 has been designed taking into account the S-DMB specifications. Therefore, there are some remarkable particularities w.r.t. the generic block presented in Figure 5. Since we have considered 4 samples per chip, the implemented block for the S-DMB receiver is composed of four parallel blocks, corresponding to each sample. Hence, we have replaced the multiplexer and the two multipliers in Figure 5 by 4 different blocks, being two arms created for each component, one for those samples multiplied
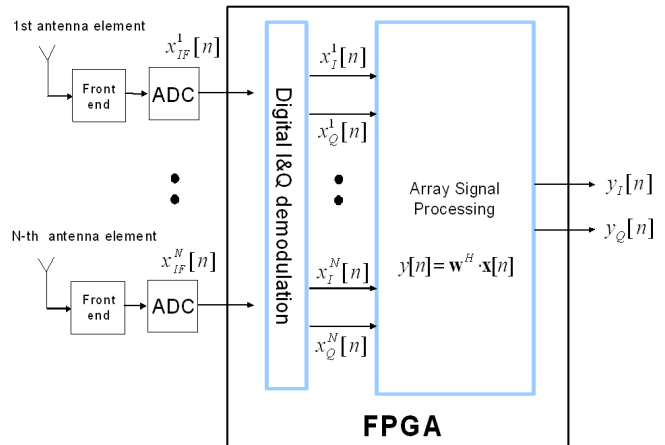


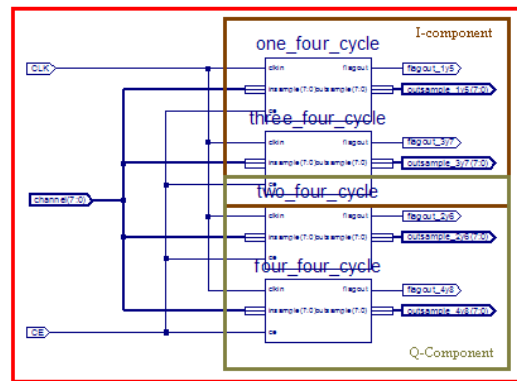Figure 6: Digital Beamforming receiver with digital I&Q demodulation.



Figure 7: Schematic of the implemented digital I&Q demodulator.

by $-1$ and another for those bypassed, operating at a frequency of $f_s/4$. In general, one can increase the granularity of the design in order to decrease the operating frequency ($f_{fpga}$) at the expenses of increasing the consumed area ($A_{fpga}$) in the FPGA, since more blocks are required. As a rule of thumb, it is considered that the following holds $f_{fpga} \cdot A_{fpga} = \kappa$, where $\kappa$ is a constant, i.e. the product defines an hyperbolic behavior. Table 1 shows $A_{fpga}$ and $f_{fpga}$ synthesis results of schematic in Figure 7 for a number of Xilinx FPGA devices. It is remarkable that not only the number of inputs are reduced, but also little computational cost is introduced by the digital I&Q demodulator w.r.t. direct downconversion strategies.

| Technology | $A_{fpga}$ (Slices) | $f_{fpga}$ (MHz) |
|---|---|---|
| XC5VLX220 | 48 of 138240 | 603.136 |
| XC4VLX200 | 37 of 89088 | 522.193 |
| XC3S1600E | 37 of 14752 | 295.513 |
| XC3S4000L | 37 of 27648 | 223.364 |

Table 1: Synthesis results of the I&Q demodulation block into different Xilinx $FPGA$ technologies.
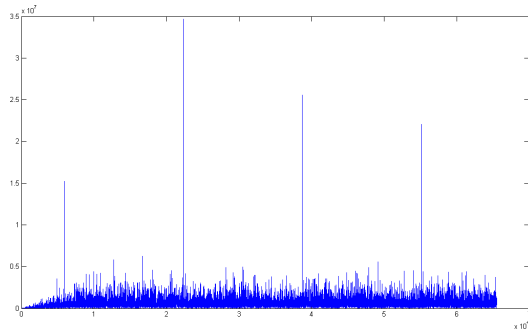
Figure 8: Correlator output without Matched Filtering after digital I&Q demodulation.
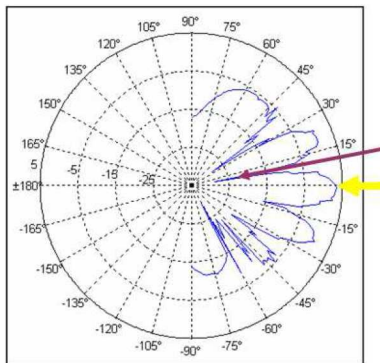


Figure 9: Radiation Pattern after Digital Beamforming: desired signal at $0^o$ and a jammer at $9^o$.

Finally, to assess the correct operation of the tested digital demodulation block, some results of the overall S-DMB receiver [9] are presented. In particular: synchronism acquisition via code correlation and pattern computation. On the one hand, Figure 8 shows the correlator output when no matched filtering is applied to the digitally demodulated I&Q components. Notice that the interference in equation (10) does not significantly affect the performance since the factor $(-1)^n$ uncorrelates this signal with the generated local CDMA code. On the other hand, the Digital Beamforming technique, namely the Temporal Reference Beamforming beamformer [8], has been implemented after digital I&Q demodulation. Basically, it uses the well-known waveform structure of a transmitted pilot signal to point the beam of the antenna array. Figure 9 shows the computed beampattern for a S-DMB signal at $0^o$ and a jammer at $9^o$. It is readily seen that the Digital Beamforming module is correctly operating, being the jammer nulled and the desired signal pointed.

## 5. CONCLUSIONS

IF sampling has emerged as a feasible and appealing strategy for SDR receivers. In this paper, a theoretical analysis has been provided along with design guidelines and the digital I&Q demodulator studied for a general antenna array receiver. In addition FPGA implementation issues were discussed, concluding that digital I&Q demodulation reduces the number of inputs to a dig-

ital signal processing device and allows high degrees of downconversion configurations. A generic block diagram has been presented, which is a straightforward implementation of the digital I&Q demodulator. As an example, it has been presented an application of those concepts to the design of a S-DMB antenna array receiver, which has been programmed in VHDL code and implemented on an FPGA device, validating the above discussions.

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