EFFECTS OF JITTER ON CONTINUOUS TIME DIGITAL SYSTEMS WITH GRANULARITY REDUCTION

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ABSTRACT

Performing digital signal processing in continuous time can be advantageous for a number of applications like biomedical implants, hearing aids, remote sensors, telecommunications, audio and speech processing. While the inherent advantages of digital implementations with respect to programmability and noise immunity are retained by this kind of signal processing, the power consumption can be much lower and the Signal to Noise Ratio (SNR) can be considerably better than for sampled data systems. The delay elements in continuous time systems must be however implemented as quasi continuous time delay lines. This is a completely different solution compared to sampled data systems and results in higher implementation costs. Furthermore the tolerances of the delay lines, mismatches between the delays of the same stage, and jitter can result in severe degradation of the system performance and must be carefully analyzed. In this contribution the effects of jitter on the signal spectrum as well as on the SNR will be considered in detail.

1. INTRODUCTION

In continuous time digital systems the signals are processed continuously in time but they are discrete in amplitude [1–6]. This new type of signal processing system requires no clock and thus the respective realizations are asynchronous [7]. Contrary to the classical asynchronous implementations however, the time interval between the samples must be also preserved, since it carries information. Therefore the delays cannot be implemented as simple binary storage elements, but must be realized as continuous time delay lines. This makes the implementation of the delay elements a critical point with respect to the required chip area and the accuracy.

Nevertheless, digital continuous time systems have some interesting properties, making them very attractive for a number of applications. Whereas the advantages of digital techniques, such as programmability and noise immunity still hold, no aliasing of out-of-band signals and quantization noise occurs due to the continuous time signal processing. Signal processing only has to be performed when signals are changing, therefore such systems have the potential for implementations which are optimized for minimum power consumption. In conventional digital systems the dominant dynamic power consumption is determined by the sampling frequency, which must be at least twice the bandwidth of the input signal. In continuous time digital systems however it is directly proportional to the spectral content of the input signal. Thus for systems which process signals with bursty traffic in real time, continuous time digital systems are especially attractive. Due to the long time periods where the signals are not changing, a tremendous potential for power consumption reduction can be expected.

In continuous time digital systems, the input analogue signals are quantized and then fed into a delta-modulator block which generates two continuous time binary signals called tokens. The first token called pulse(t_i) indicates that the signal has changed by one quantization level at time instant t_i. The second token is an up-down indicator u$/$d(t_i) which gives the direction of the change. These continuous time signals can be directed to delay elements to perform digital signal processing. While in sampled data systems, simple RAM cells can be used for the implementation of the delay cells, the realization in continuous time DSP systems is more complex, since they must be implemented as continuous time delay lines. Each binary delay line is composed of a chain of N_{del} basic delay cells, as shown in fig. 1. For a sinusoidal signal with an amplitude of 1, maximum frequency of $f_{\text{in,max}}$ and N quantization bits, the shortest time interval T_{gran}, during which the signal can increase or decrease by one quantization level is given by [8]:

$$T_{\text{gran}} = \frac{1}{2^{N-1} \cdot 2\pi f_{\text{in,max}}} \tag{1}$$

A continuous time delay element of delay T_D can be thus implemented by a cascade connection of N_{del} basic delay cells, each generating a delay of T_{gran}. The basic delay cells shown in fig. 1 consist of a delaying element (Δ) which delays the pulse(t_i) and a flip flop storing the up-down information u$/$d(t_i). In [8] the implementation of such a delay element is described in more detail, where a capacitor and a current source were used for the adjustment of the delay time. Furthermore, a handshaking mechanism is implemented between the basic delay cells in order to guarantee an error free operation of the delay line.

In [9], a method for the reduction of the hardware complexity of continuous time digital systems was proposed. It was shown that the granularity and therewith the implementation costs of the delay elements can be reduced by a factor of 4 without severe performance degradation. Furthermore it was proposed to implement the delay elements in a parallel structure which can result in further savings. In parallel structures however, signals are processed in different branches and therefore jitter between the signals in the parallel branches may degrade the system performance. In this

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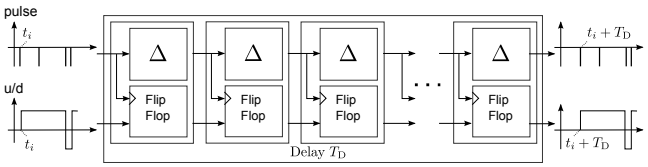

Figure 1: Serial continuous time delay element with delay time T_D consisting of N_{del} cascaded basic delay cells.

contribution, the effects of jitter on the signal spectrum as well as on the SNR of the signals in continuous time systems with and without granularity reduction will be investigated.

In section 2, the implementation of the parallel delay elements is reviewed. In section 3 the effects of jitter as well as the concept of granularity reduction is explained. Section 4 gives a mathematical model for jitter. Finally in section 5 the simulation results are presented.

2. CONTINUOUS TIME DELAY ELEMENTS IN PARALLEL STRUCTURES

Fig. 2 shows a delay element with parallel structure where each pulse is delayed by a different basic delay cell. It implements a First In First Out (FIFO) structure with N_{del} sets, where each set contains a basic delay cell providing a pulse delay of T_D, and a RAM cell holding the up/down information. Whenever a new data token arrives at the input, it is routed by the control logic to an unoccupied set of delay/RAM cells. This cell becomes the newest active set. After a delay time T_D, the respective cell generates a new pulse at the output, accompanied by the corresponding up/down information. This way, the complete delay element can contain up to N_{del} pulses at the same time.

The basic delay cell has a simple circuit structure which consists of a capacitor that is charged by a current source. The delay time T_D is determined by the charging time of the capacitor. The comparator needed to detect the switching level of the capacitor voltage can be shared among the basic delay cells, as the delays of cells expire one at a time, in the order of pulse arrivals. This can easily be managed by the FIFO control logic. For proper operation of the multiplexing circuitry, it is necessary that the delay through the control logic, the analogue multiplexer and the comparator is smaller than the shortest possible interval between successive pulses (T_{gran}). Whereas the delay time of the basic delay cell of the serial structure in fig. 1 is T_{gran}, it is increased to T_D for the basic delay cell of the parallel structure. Therefore the capacitance must be increased and/or the charging current must be decreased.

The chip area, the power consumption and the delay precision are the key factors for the delay elements. For a first rough comparison of chip area and power consumption of the two approaches, we assume that the circuit must process signals with a given granularity T_{gran}. For the parallel implementation the minimum number of delay/RAM cell sets required for generation of a delay T_D is $N_{del} = T_D/T_{gran}$. This is the same as the number of stages in the serial structure if the stage delay is set to T_{gran}. Thus the delay/RAM cell set can be compared directly with a basic serial delay stage. Due to the smaller number of comparators and the reduced charging currents, the parallel structure can be expected to

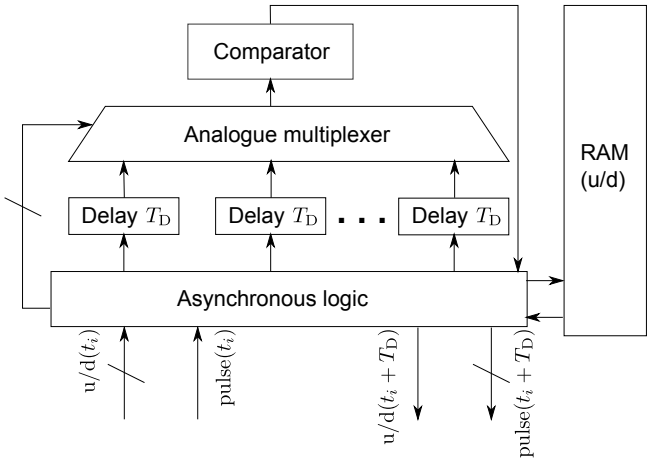

Figure 2: Continuous time delay element with delay time T_D consisting of N_{del} parallel basic cells.

consume considerably less power than the serial one. The increased chip size due to the larger capacitors in the parallel implementation is expected to be larger than the size of the N_{del} comparators required in the serial implementation. On the other hand the chip area is reduced since the handshaking logic is not required for the parallel structures. Thus the required area can be estimated to be about the same for both structures.

With respect to delay precision, both approaches depend in the same way on the underlying semiconductor manufacturing process to create matched devices which is in this case, capacitors and transistors giving the current sources. The absolute precision of delays is not as important as the matching of delays in a filter. Deviations from the correct absolute value will result in an (often acceptable) scaling of the filter cutoff frequency, whereas delay mismatch can severely degrade the filter characteristic. In the serial implementation all pulses will take the same path through the delay element, thus device matching may be good enough for many applications. In a parallel delay element however the paths taken by the pulses are different. A delay mismatch between these paths adds jitter to the output pulses. This jitter of the delay time is a key issue of the parallel architecture.

From the circuit design perspective, the high matching requirements limit the degree to which charging currents can be reduced. This is because the matching of currents becomes more difficult as currents decrease below 1μA. In [8], it was proposed to calibrate a serial delay element, using a delay locked loop and an external reference clock signal. For the parallel delay elements, a similar calibration must be applied to each individual delay cell to reduce jitter amplitude. Since the charging currents can be reduced by calibration, the size of capacitors may also be reduced. Calibration and other jitter reduction techniques are currently under investigation.

3. EFFECTS OF JITTER ON CONTINUOUS TIME SYSTEMS

As has been shown in section 2, each branch of a delay element with parallel structure, stores data tokens with different time offsets. The maximum amount of jitter which can be tolerated is thus one of the key parameters for the implementation of such continuous time delay elements. In order to

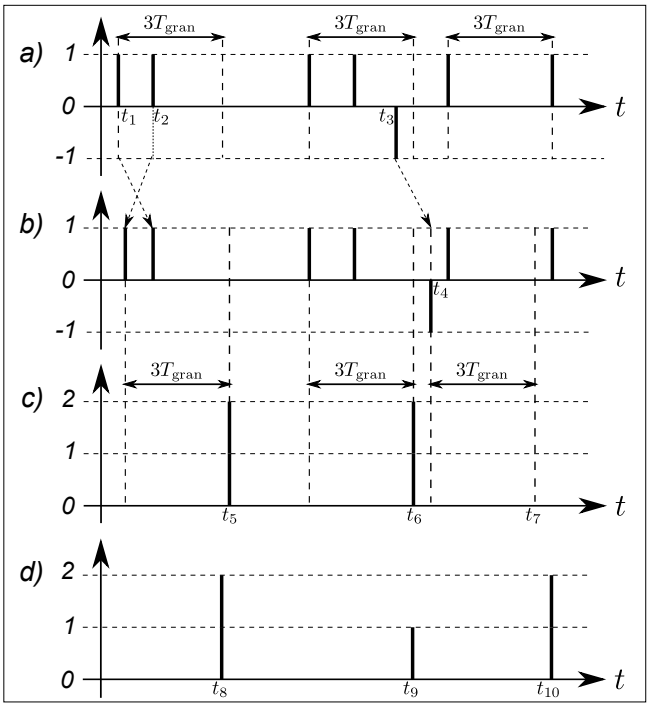

Figure 3: An example of a sequence of data tokens in a continuous time system a) full granularity without jitter, b) full granularity with jitter, c) reduced granularity with jitter, d) reduced granularity without jitter.

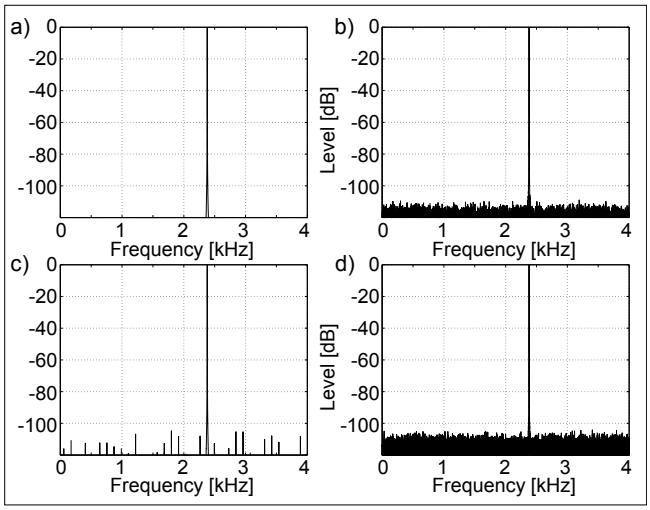

Figure 4: Spectra of quantized, continuous time sinusoidal signals, a) Full granularity without jitter, b) full granularity with jitter, c) reduced granularity without jitter, d) reduced granularity with jitter.

evaluate the performance of the signal processing in continuous time systems, the properties of a quantized sinusoidal signal, processed by a continuous time delay element will be analyzed in the following. The SNR, obtained in the band of interest, will be determined for sinusoidal signals of different frequencies. Furthermore, the performance degradation due to the jitter and granularity reduction will be evaluated.

In [3] it was shown that a delta modulator used for A/D-conversion in continuous time systems generates output tokens, signaling a change and the direction of the change in the original signal. In order to simplify the explanation each token is chosen to be either 1 or -1, representing both the change and the direction of the change in one place [9].

Fig. 3 shows a sequence of randomly selected data tokens. In fig. 3a an example of the output of a delta-modulator is given, where no jitter or granularity reduction is applied. Fig. 3b shows a possible scenario for the jittered signal where the first two tokens at time instants t_1 and t_2 are swapped and the token at time instant t_3 is shifted to t_4 which may lead to a degradation of the SNR.

In a system with reduced granularity, a certain number of tokens will be summed up in fixed time intervals and replaced by the resulting sum. This will reduce the total number of tokens and consequently the hardware complexity and power dissipation. Fig. 3d shows the granularity reduced version of the original signal from fig. 3a, where tokens are divided into several granularity groups, each having a duration of $3T_{\text{gran}}$. For the first granularity group, the summation starts at t_1 and all the tokens until the time instant $t_1 + 3T_{\text{gran}}$ are summed up. As the minimum distance between adjacent tokens is T_{gran}, the maximum number of tokens which may fit into one granularity group is 4, which is called the granularity reduction factor.

Fig. 3c shows the granularity reduced signal again, but this time generated from the jittered version of the input signal from fig. 3b. As can be seen in the diagram, the jitter which occurs at t_3, changes the structure of the last two granularity groups. As the jittered token appears at t_4, it will be also summed up in the last group leading to different results.

In order to analyze the effects of jitter on the spectrum of the input signal, jitter was modeled as a uniform distributed random variable. Fig. 4 shows the spectra of the reconstructed sinusoids with full and reduced granularity, as well as with and without jitter, where the maximum jitter of the tokens was chosen to be less than 50% of T_{gran} and a granularity reduction by a factor of 4 was assumed. The band of interest is assumed to extend from 0 to $f_{\text{in,max}} = 4$kHz.

For sinusoids with frequencies larger than $\frac{1}{3} f_{\text{in,max}}$, the 3rd and higher order harmonics, which are generated by the quantization operation, are located above the band of interest which results in a considerably improved SNR. While increasing the input frequency further up to 4 kHz, and keeping the jitter to less than 50% of T_{gran}, only the white noise floor increases. As shown in fig. 4a and 4c, in a system without jitter, granularity reduction increases the noise level slightly. Fig. 4b and 4d also show the same result for a system with jitter (less than 50% of T_{gran}). These results confirm that the SNR is only slightly degraded if the jitter is smaller than 50% of T_{gran}.

If the jitter is however increased to above 50% of T_{gran}, the noise level for the lower frequency components may increase considerably for sinusoids with frequencies larger than $\frac{3}{4} f_{\text{in,max}}$. Fig. 5 shows this effect for an input sinusoid with a frequency of 3.3kHz. This holds for both full and reduced granularity systems. The significant degradation of the SNR for sinusoidal signals with higher input frequencies is due to the fact that the generated tokens are placed close to each other and adjacent tokens may be swapped and destroy the signal shape as was explained in fig. 3.

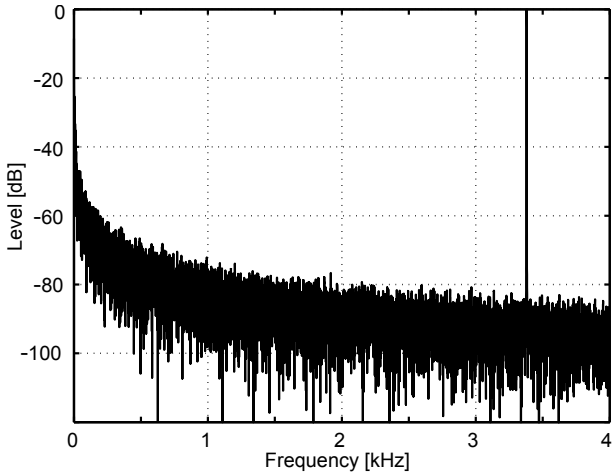

Figure 5: Spectrum of a quantized, continuous time sinusoidal signal for a system with jitter larger than 50% of T_{gran} and input frequency of 3.3kHz.

4. A MATHEMATICAL MODEL FOR JITTER IN CONTINUOUS TIME DIGITAL SYSTEMS

The sinusoidal input signal $x(t)$ and the respective quantized signal $q(t)$ can be described as follows:

$$x(t) = \sin(2\pi f t); \quad t \in \mathbb{R}^+ \cup \{0\},\ f \in [0, f_{\text{in,max}}], \qquad (2)$$

$$q(t) = \text{sign}(x(t)) \cdot \alpha \left\lfloor \frac{|x(t)|}{\alpha} + \frac{1}{2} \right\rfloor. \qquad (3)$$

In equation (3), sign() is the sign function, and $\lfloor\rfloor$ and $||$ are the floor and absolute value operators respectively. As the amplitude of $x(t)$ is 1, the quantization step size is given by $\alpha = 1/2^{N-1}$ where N is the number of quantization bits.

The tokens, which are generated by a delta modulator and jittered by the delay element, are modeled as:

$$d(t) = \sum_{i=0}^{+\infty} (q(t_{i+1}) - q(t_i))\delta(t - t_{i+1} + P_{i+1}),$$

where $\delta()$ is the Dirac delta function and the jitter for the i^{th} token is modeled as the random variable P_i with $\text{E}(P_i) = 0$.

The maximum rate of change for input signal $x(t)$ from equation (2) is given by $2\pi f$ [8]. Therefore the maximum error which is caused by a random variable P_i for token i and input frequency f is given by:

$$e_{i,f,\text{max}} = 2\pi f P_i.$$

The maximum error for the highest allowed input frequency $f_{\text{in,max}}$ is obtained by using equation (1):

$$\begin{aligned} e_{i,\text{max}} &= 2\pi f_{\text{in,max}} P_i = 2\pi \frac{1}{T_{\text{gran}} \pi 2^N} P_i \\ &= \frac{P_i}{T_{\text{gran}} 2^{N-1}} = \frac{P_i}{T_{\text{gran}}} \alpha, \end{aligned}$$

where α is the quantization step size. If the jitter increases to 50% of T_{gran} we have:

$$e_{i,\text{max}} = \frac{T_{\text{gran}}/2}{T_{\text{gran}}} \alpha = \alpha/2.$$

Thus for a delay element with parallel structure and a maximum jitter higher than 50% of T_{gran}, adjacent signal levels may be shifted by $\alpha/2$ towards each other since the P_i's are independent random variables. In this case, the SNR is significantly degraded.

5. SIMULATION RESULTS

For the simulations, sinusoidal signals with an amplitude of almost 1 and a maximum input frequency of 4kHz were used. The quantization was performed with $N = 8$ bits, leading to a granularity duration of about $T_{\text{gran}} = 314$ns from equation (1). The quantized signal was fed to a delta-modulator and optionally a granularity reduction module, generating jittered tokens, where the jitter was modeled as a uniform random variable. The SNR was determined from the reconstructed signal where systems with full granularity as well as with reduced granularity were considered. Fig. 6 shows the complete simulation chain.

As seen in fig. 7 and explained in section 3, in a full granularity system with a jitter of less than 50% of T_{gran} (150ns in our case), the SNR improves with increasing input frequency up to 1.34kHz, since the harmonics are shifted out of the band of interest. Above this frequency, the SNR drops again, since the white noise floor is also increased with increasing frequency. For a jitter larger than 50% of T_{gran} the SNR is reduced drastically for higher input frequencies.

Fig. 8 shows the SNR diagram for a sinusoidal signal with the same parameters, but with granularity reduction by a factor of 4. As seen in the figure and explained in section 3, the SNR decreases slightly compared to a system with full granularity. A large jitter has similar effects for higher frequencies as for the system with full granularity.

In general, for both systems with and without granularity reduction, if the jitter stays below 50% of T_{gran} (150ns in our scenario) the SNR is better than 70dB. Thus a reliable implementation can be obtained by keeping the jitter below a well defined limit.

6. CONCLUSION

In continuous time systems the implementation of the delay elements is a very critical point with respect to the required chip area and the power consumption. Recently, novel continuous time delay elements were proposed based on parallel structures and granularity reduction. Using these elements the chip area and the power consumption can be significantly reduced without sacrificing performance. The main challenge for the implementation of these novel elements is however the jitter which results from the fact that the tokens are processed in different branches simultaneously when using parallel delay elements. Thus, in this contribution, the effects of the jitter were investigated in detail for systems with full and reduced granularity.

The simulation results confirmed that a jitter lower than 50% of T_{gran} results in an acceptable performance when using these new structures. It turned out that the SNR of the output signal was better than 70dB in our scenario, even if

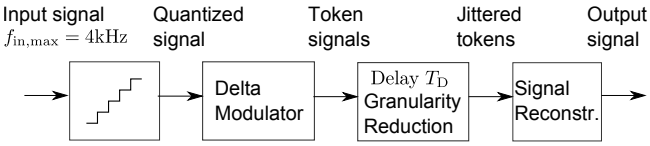

Figure 6: Simulation chain for a continuous time delta modulator with jitter and granularity reduction

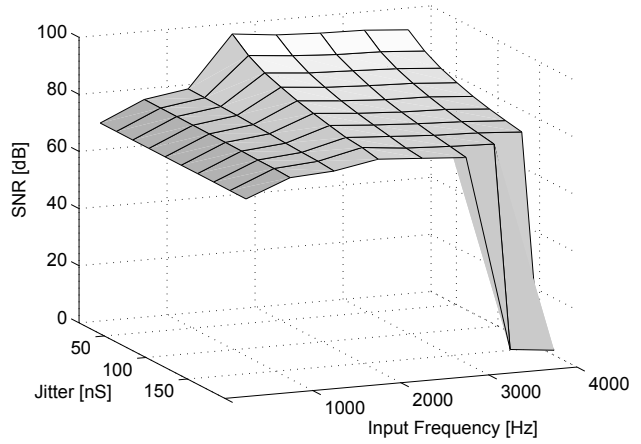

Figure 7: SNR of a sinusoidal signal with full granularity, processed by a continuous time system with jitter.

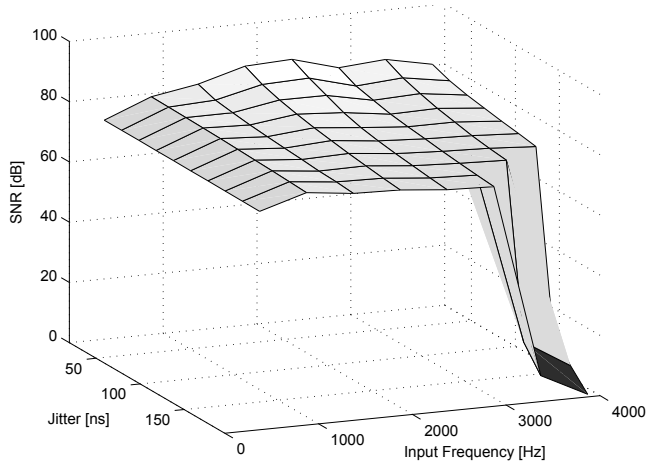

Figure 8: SNR of a sinusoidal signal with reduced granularity, processed by a continuous time system with jitter.

a granularity reduction by a factor of 4 was applied. This SNR range offers an acceptable performance, e.g. for speech processing and other applications.

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