A HIGH-PERFORMANCE ARCHITECTURE OF JPEG2000 ENCODER

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ABSTRACT

This article presents hardware architecture of JPEG2000 encoder core, oriented for HD video broadcast and surveillance applications. Thanks to developed efficient 2-D DWT engine that is capable of computing four coefficients per clock cycle, and adopted two EBCOT TIER-1 modules, with smart switching of the channels, the maximum compression speed of 180 Msamples/s at 100 MHz, in lossy mode is achieved. The architecture is implemented in VHDL and synthesised for FPGA devices, and ASIC 0.13 μm CMOS technology. Performance simulations, conducted on a set of natural images and video sequences, have revealed that the encoder is capable of processing 1080p 4:4:4 signal with a speed of 30 frames per second. Additionally, an excellent quality of reconstructed images has been observed, with respect to the reference, software encoder.

1. INTRODUCTION

In the age of acquisition and processing of high resolution images and video, efficient systems of signal compression-decompression play a fundamental role. This issue is extremely important in the case of 3D video signals, where simultaneous processing of more than one frame is assumed. Present multimedia applications require also resolution and quality scalability, flexible rate control, region of interest coding, increased colour depth, error resilience and other demanding features. JPEG2000 still-image compression standard [1][2], which outperforms significantly JPEG standard, meets all these demands in a single codestream. Thanks to many sophisticated coding tools, such as discrete wavelet transformation (DWT) and two-tiered embedded block coding with optimized truncation (EBCOT) [3], it allows to obtain excellent compression performance and is commonly used in digital cinema (DCI) and HDTV applications.

By efficiency of a compression system we mean its extensive processing power. Nowadays, the requested throughput of video encoders is so enormous that use of their software implementations is out of the question in real-time applications. The only solution for a high speed, low latency realisations of complex image encoding algorithms are specialized hardware implementations. Obviously, the superior throughput of hardware solutions is always balanced by FPGA or ASIC area resources and power consumption. In the literature, several architectures of high-performance JPEG2000 encoder have been proposed [4-11]. All these implementations meet different design challenges that the researchers try to overcome. Firstly, the mismatch between word-based DWT dataflow and sequential, computational intensive bit-plane processing of EBCOT algorithm requires significant amount of on-chip memory resources or high external memory bandwidth, to buffer data, passed between these two blocks. Secondly, an entropy coding algorithm in JPEG2000 requires sophisticated control mechanisms and many branching conditions. In hardware it results in complex, combinatorial logic and considerable length of the critical paths. The design maximum frequency is also deteriorated due to long arithmetic paths in the DWT processor. Finally, an enormous complexity of JPEG2000 compression algorithms, which enforces use of pipeline computations, reflects in significant area of the encoder chip.

In this work we propose a high performance, hardware architecture of JPEG2000 encoder targeted for HD image resolutions. High throughput of the presented design is achieved by two main strategies. Firstly, very efficient 2-D DWT engine that computes four coefficients per one clock cycle is applied in the encoder. Secondly, parallel processing of subbands is obtained through exploiting two channels of EBCOT TIER-1 module, with a smart switching technique. What is more, single TIER-1 module incorporates several techniques of fast and efficient entropy coding, elaborated for the base JPEG2000 design [12-14]. The encoder utilizes external SDRAM memory to store intermediate, compression results, what minimizes the internal memory resources and enables realisation of the pipelining at a frame level. All these issues, together with improved external memory access scheduling, result in a compression performance that meets requirements of real-time HDTV applications. The rest of this paper is organized as follows. Section 2 contains a brief description of JPEG2000 coding tools. Proposed architecture of the JPEG2000 encoder together with performance improvement strategies are shown in Section 3. Implementations results, performance measurements and comparisons with competitive solutions are gathered in Section 4. Finally, conclusions and future work aspects are summarized in Section 5.

2. JPEG2000 OVERVIEW

The block diagram of JPEG2000 encoder is presented in Figure 1. Input image components are firstly pre-processed by conducting DC level shifting and multiple component transform on the samples. The image plane is partitioned into rectangular, non-overlapping tiles, which are compressed independently. Each tile is decomposed by discrete wavelet transformation into subbands with a certain number of decomposition levels. DWT coefficients are then uniformly quantized, to be further partitioned into code-blocks. The entropy coder processes the bit-planes of coefficients in the code-block, to form the output JPEG2000 codestream [2].

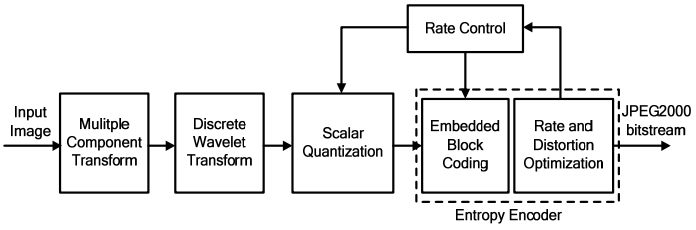

Figure 1 – Block diagram of JPEG2000 encoder.

Rate controller, and rate-distortion optimization blocks are not directly standardised in the norm, however they are given informative and pose an important part of the encoder.

2.1 Multiple Component Transform

JPEG2000 standard enables compression of multiple-component images (e.g. RGB, YC_bC_r) of arbitrary bit-depths. To provide better compression efficiency the standard defines two types of de-correlating transformation derived on the first three input image components. These are reversible component transform (RCT) Eq.1, used in lossless compression mode and irreversible component transform (ICT) Eq.2, utilized in lossy mode. Prior to computation of the transformations, DC level shifting on input samples is performed, in the case of their unsigned representation.

$$\begin{aligned} Y &= 0.299R + 0.587G + 0.114B \\ C_b &= -0.16875R - 0.33126G + 0.5B \\ C_r &= 0.5R - 0.41869G - 0.08131B \end{aligned} \quad (1) \qquad \begin{aligned} Y &= \left\lfloor \frac{R + 2G + B}{4} \right\rfloor \\ C_b &= R - G \\ C_r &= B - G \end{aligned} \quad (2)$$

Y denotes here luminance component, whereas C_b, C_r are chrominance components.

2.2 Discrete Wavelet Transform

Input image, after MCT transform is partitioned into rectangular, non-overlapping blocks – so-called tiles, which in turn are processed independently by discrete wavelet transform algorithm. DWT applied in JPEG2000 is a two-dimensional (2-D), multi-level filtering method that consists of two 1-D filtering operations performed in vertical and horizontal directions respectively [2]. Each 1-D wavelet transform decomposes array of samples into low-pass set – downsampled, low-resolution approximation of the original signal, and high-pass set – downsampled residuum of the original signal. As a result of DWT decomposition, the tile is divided into four subbands – *LL, HL, LH, HH*, which contain transform coefficients with different horizontal and vertical spatial frequency characteristics. The LL subband can be further, recursively decomposed in a dyadic fashion. As an example three-level DWT decomposition, which results in 10 subbands is presented in Figure 2.

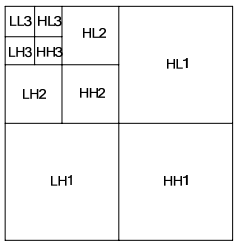

Figure 2 – Three-level DWT decomposition of image tile.

JPEG2000 defines both irreversible and reversible discrete wavelet transformation. The first one is implemented as 9/7-tap Daubechies filter [2], whereas the second is implemented by means of 5/3-tap filter. The filters can be implemented in a convolution-based or a lifting-based fashion, with symmetric extensions of the samples at the signal boundaries. In hardware realisations, the most popular is a lifting approach, which has many advantages over traditional FIR filtering [15]. It is also recommended in the JPEG2000 standard. Irreversible DWT in JPEG2000 consists of four lifting steps and two scaling steps as it is presented in Eq.3.

$$\begin{cases} Y(2n+1) = X_{ext}(2n+1) + \alpha(X_{ext}(2n) + X_{ext}(2n+2)) & step1 \\ Y(2n) = X_{ext}(2n) + \beta(Y(2n-1) + Y(2n+1)) & step2 \\ Y(2n+1) = Y(2n+1) + \gamma(Y(2n) + Y(2n+2)) & step3 \\ Y(2n) = Y(2n) + \delta(Y(2n-1) + Y(2n+1)) & step4 \\ Y(2n+1) = KY(2n+1) & step5 \\ Y(2n) = (1/K)Y(2n) & step6 \end{cases} \quad (3)$$

α, β, γ, δ denote lifting coefficients, K is a scaling factor and $X_{ext}(2n)$, $X_{ext}(2n+1)$ represent even and odd samples of input, boundary extended signal. Reversible DWT consists of only two lifting steps. High-pass and low-pass coefficients are calculated using following equations:

$$\begin{aligned} Y(2n+1) &= X_{ext}(2n+1) - \left\lfloor \frac{X_{ext}(2n) + X_{ext}(2n+2)}{2} \right\rfloor \\ Y(2n) &= X_{ext}(2n) + \left\lfloor \frac{Y(2n-1) + Y(2n+1) + 2}{4} \right\rfloor \end{aligned} \quad (4)$$

2.3 Quantization

After discrete wavelet transform, the dynamic range of coefficients is decreased by scalar quantization process. The only exception is lossless compression mode, where the quantization step is equal 1. In other case, subband DWT coefficients – $a_b(u,v)$, are quantized according to Eq.5:

$$q_b(u,v) = sign(a_b(u,v)) \left\lfloor \frac{|a_b(u,v)|}{\Delta_b} \right\rfloor \qquad \Delta_b = 2^{R_b - \varepsilon_b}\left(1 + \frac{\mu_b}{2^{11}}\right) \quad (5)$$

Δ_b represents quantization step of a particular subband and R_b denotes dynamic range of the coefficients, which is dependent of image component bit depth and type of the subband (*LL, HL, LH* or *HH*). ε_b, μ_b are the quantization step's exponent and mantissa respectively. Quantized coefficients are passed to entropy coding algorithm in a sign-magnitude representation.

2.4 Embedded Block Coding

The embedded block coding in JPEG2000 is divided into two parts – TIER-1 and TIER-2. During TIER-1 coding, each subband, containing quantized DWT coefficients is partitioned into rectangular code-blocks, whose dimensions must be power of two. In Figure 3, there is presented an example of subband decomposition into sixteen code-blocks of size 64x64, and further layers of the entropy coding algorithm – bit-planes and stripes. The bit-planes are processed from the most significant one (containing non-zero element) to the least significant one. Each bit of the analyzed bit-plane is encoded by one of the three coding passes called: significant propagation, magnitude refinement and clean-up [1][2]. The coding passes utilize a special scan order to process the stripes. As a result of bit-plane coding, a pair of context and binary decision values is generated for each bit position, and given at the input of MQ-encoder, adopted in the JPEG2000 standard. The context data generated by bit-plane coder is used to derive the estimated probability value, from the predefined look-up table with 47 entries. Code-bytes obtained from arithmetic encoder are distributed across one or more layers within the codestream [2]. Each layer successively contributes a certain level of improvement into reconstructed image. Code data representing a specific tile, layer, component and resolution form packets.

TIER-2 algorithm holds the process of final codestream generation. It is done by formation of several headers (main header, tile

headers etc.), with special markers and marker segments, and incorporating code-bytes collected in the packets. These can be put into codestream in five different orders, what is defined in the standard as a progression order [1][2].

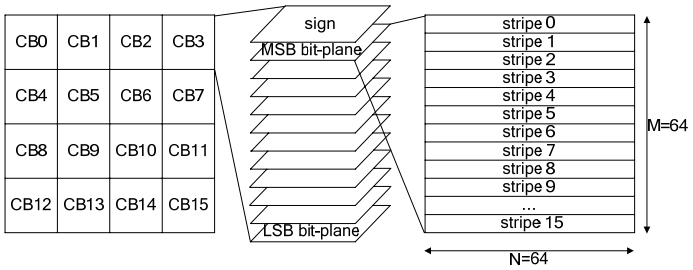

Figure 3 – Different coding levels of EBCOT algorithm (assumed code-block size is 64x64).

3. PROPOSED ENCODER ARCHITECTURE

Figure 4 presents block diagram of the proposed, high-performance JPEG2000 encoder. It consists of interface controller module, multiple component transform (MCT) module, discrete wavelet transform engine (DSP), DWT coefficients de-multiplexer (CHANNEL DMUX), two EBCOT TIER-1 modules, EBCOT TIER-2 stream formatter and memory management units: TIER-1 MMU, TIER-2 MMU, external memory scheduler. Configuration of the encoder is performed via interface controller block. It communicates with a master device using three interfaces. Interrupts interface informs about compression state within the encoder. Configuration interface enables setting of the compression parameters such as decomposition levels, code-block size, tile size, filter mode and etc. Codestream interface is a JP2 stream output. Despite communication with external host, the interface controller provides synchronization and enables processing in the encoder sub-modules (MCT, DSP, EBCOT). Intermediate results of the compression algorithm are buffered in the external SDRAM memory, what significantly decreases on-chip memory resources and enables pipelining of MCT, TIER-1 and TIER-2 operations at a frame level. The external memory bandwidth is effectively utilized thanks to the memory scheduler block, synchronized by 200 MHz memory clock pulse – *clk_mem*. Description of the modules implementing JPEG2000 coding algorithms is presented in the following subsections.

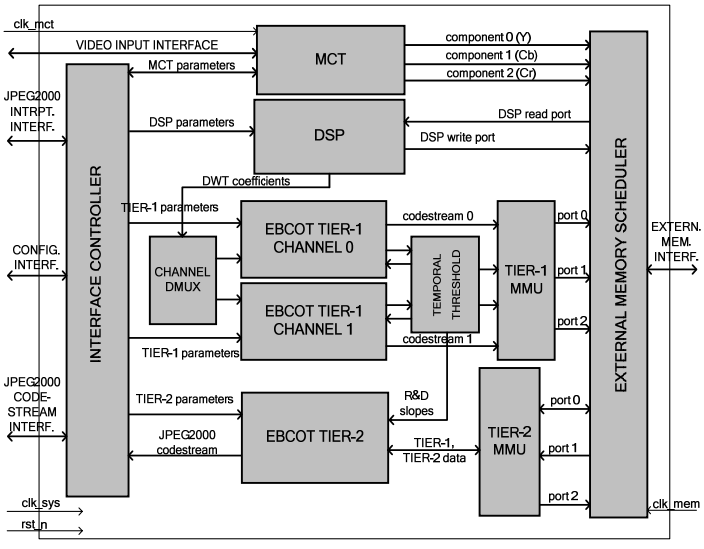

Figure 4 – Block diagram of the proposed JPEG2000 encoder.

3.1 MCT Module

Input image samples are transferred directly to multiple component transform module through video input interface, synchronized by separate, 200 MHz clock signal – *clk_mct*. The module performs DC level shifting and then applies reversible component transform or irreversible component transform according to Eq. 1 and Eq. 2. Internal architecture of the module is two-level pipelined in order to decrease critical path. Obtained YC_bC_r coefficients are buffered in the external memory, to be further processed by DSP block.

3.2 DSP Module

DSP module is an implementation of discrete wavelet transformation and quantization algorithms. The module performs multi-level, two-dimensional reversible or irreversible transform, with symmetric boundary extension. Presented encoder provides up to five DWT levels in lossy compression and up to seven levels in lossless mode. The DSP block consists of four sub-modules as presented in Figure 5. The sub-modules take at the input a compression parameters set, asserted by interface controller module.

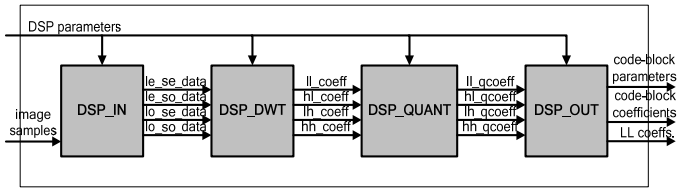

Figure 5 – Internal structure of DSP block.

The first, DSP_IN block is a tile formatter. It reads blocks of 136x136 image samples (128x128 with four samples of the overlap on each boundary), from the external memory utilizing memory scheduler. Then, it sends to DWT processor four samples simultaneously: even sample from even line – *le_se_data*, odd sample from even line – *le_so_data*, even sample from odd line – *lo_se_data*, and odd sample from odd line – *lo_so_data*. In the case of DWT levels greater than 1, blocks of *LL* subband samples are read from the external memory to provide further decompositions.

DSP_DWT is an efficient implementation of the 2-D discrete wavelet transform. The two-dimensional filtering is partitioned into two vertical 1-D (performed first) and two horizontal 1-D, lifting-based transform engines. Such a structure, depicted in Figure 6, after a latency of four image lines, allows to obtain four DWT coefficients (from *LL, HL, LH* and *HH* subband respectively) in a one clock-cycle. Each 1-D DWT processor has eight-level pipeline, optimized to minimize rounding error between the stages. The proposed DWT module enables 5/3-tap and 9/7-tap filtering in the same hardware architecture. Choice of the transform type is programmable. When reversible transform is enabled, the result coefficients are taken from the fourth stage of the pipeline. Before sending DWT coefficients to the output, the data are scaled according to steps 5-6 of Eq.3. DSP_DWT block can process incoming samples with a maximum throughput of 800 Msamples/s, when synchronized by 200 MHz clock pulse. In the presented encoder the performance is equal 400 Msamples/s, assuming 100 MHz pixel clock. DSP_QUANT sub-module is a straightforward implementation of the scalar quantization applied in ISO/IEC 15444-1 standard. The block performs simultaneous quantization of four input coefficients, derived for all DWT subbands. The quantization process is three-level pipelined, with the stages that correspond to Eq.5 formula.

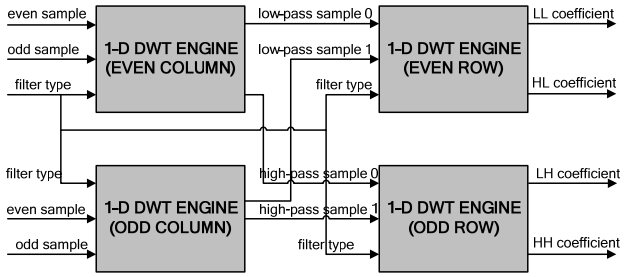

Figure 6 – Block diagram of the applied 2-D DWT engine.

Values of the exponent and mantissa, for each DWT level and each subband, are loaded to DSP_QUANT during configuration of the encoder, and stored in the internal memory. The quantization parameters are derived in software and transmitted to the encoder as the compression parameters.

DSP_OUT sub-module provides an interface between word-based DWT dataflow and a bit-plane wise entropy coding. It takes coefficients from the quantization block and writes them into four, doubled, on-chip memories of 2x64x16 size. At each memory word four consecutive, quantized coefficients are stored. Due to implemented mechanism of double buffering, the first half of the subband memory can be written, whereas the second is ready to be read. Buffered coefficients are grouped into code-blocks units and then successively transmitted to the EBCOT engine. Presented design supports code-blocks of maximum size up to 64x64. In the case, when multi-level DWT transform is applied, *LL* coefficients are written back to the external memory for further processing.

3.3 EBCOT TIER-1 Channels and Rate Control

Embedded block coding with optimized truncation is the most computationally intensive part of the JPEG2000 compression standard and is a bottleneck of the encoder architecture. Informative block diagram of the applied EBCOT TIER-1 module is depicted in Figure 7. Bit-plane coder (EBC_BPC) is the first stage of EBCOT algorithm. It takes at the input code-block coefficients and generates context-symbol pairs, passed further to binary encoder (CABAC). Consecutive bit-planes are scanned in three coding passes, called significance propagation, magnitude refinement and cleanup. From the perspective of the rate control algorithm, each pass can be understood as quality improvement (reduction of distortion) in the reconstructed image [14]. EBC_CABAC is the next sub-module of TIER-1 processing path. The block is a smart implementation of context adaptive binary arithmetic coder, with an ability to encode two symbols per a clock cycle, and implemented mechanism of inverse multiple branch selection (IMBS) [12][14] to shorten the critical path. Obtained code bytes can be truncated at some rates that correspond to each coding pass. Calculation of truncation points length is carried out in EBC_RATE. Distortion information, generated by the bit-plane coder, and truncation lengths, derived by EBC_RATE are transferred to CONVEX_HULL analysis module. Here *Δ distortion / Δ rate* slopes are calculated, which in turn, are the basis of Discrete Lagrange Optimisation performed in TEMPORAL THRESHOLD module. Truncated codestreams that have the smallest slopes, but greater than the temporal threshold, are optimal in the sense of rate-distortion criteria [14] and form output JP2 stream. The threshold is updated for the consecutive frames of compressed image sequence, by exploiting the value from preceding frame, to shorten the overall compression time. In the case when calculated slope is less than the threshold, a termination signal is passed to EBC_BPC to end code-block processing at current coding pass.

Maximum performance of single EBCOT TIER-1 channel is approximately 50 Msamples/s at 100 MHz, in lossless compression mode. To increase the encoder performance we propose to incorporate two such TIER-1 channels. This solution is beneficial because processing of *HL, LH* and *HH* subbands is significantly shorter, than compression of *LL* subband. It can be explained by residual, low-amplitude content in the high-pass code-blocks, being in contrast to low-pass, high-amplitude coefficients observed in the *LL* code-blocks. Conducted experiments revealed that during *LL* subband processing, by first TIER-1 channel, the second block is capable of compressing both *HL* and *LH* subbands. Then, only *HH* subband is left for processing, what can be done by either channel 0 or channel 1, depending of the end of coding order. Compression of *HH* subband is extremely rapid, comparing to other subbands.

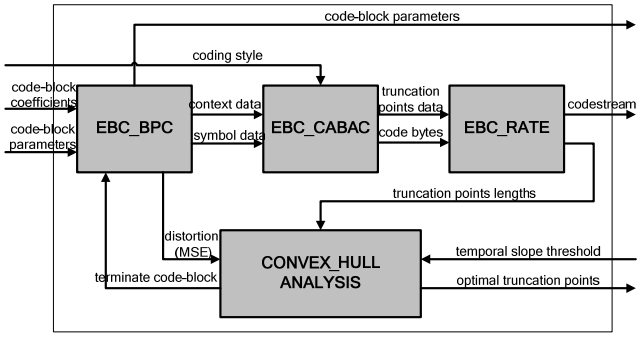

Figure 7 – Internal structure of EBCOT TIER-1 module.

3.4 EBCOT TIER-2 Module

EBCOT TIER-2 module implements final stage of the compression process. It performs sequence of tasks to form the final JPEG2000 codestream. When TIER-1 processing of all code-blocks ends, the TIER-2 module initiates second part of the rate control algorithm. It relies on accurate selection of truncation points rates that meet target bit-rate constraint. Next, the module starts producing JP2 stream, consisting of several headers and block-coded data assembled in contiguous segments – packets. The module supports two (component-resolution and resolution-component) progression orders from five defined in JPEG2000 standard. The packets are coded with a use of bit-stuffing technique and utilizing hierarchical tag trees to effectively create reduced-resolution levels of data arrays [14]. Typical, operating frequency of EBCOT TIER-2 module is 100 MHz, however it can be synchronized by maximum 150 MHz clock pulse.

4. IMPLEMENTATION RESULTS, PERFORMANCE

The JPEG2000 encoder design was implemented in VHDL hardware description language and synthesised for FPGA devices and ASIC technology. The encoder was configured to compress images of resolution up to 2048x2048 and pixel components dynamic range of 8-bit per sample. Maximum allowed tile size is equal 2048x2048. Such a configuration requires 64 MB of the external SDRAM memory. The core was extensively verified using our hardware-software verification platform. Its compression efficiency has been evaluated, by utilizing a repository of HD test images of 1280x720 and 1920x1080 resolutions, encoded with different parameter sets. Implementation results for Xilinx Virtex-5, Altera Stratix III FPGAs and TSMC 0.13 µm CMOS process are presented in Table 1. For the needs of comparison with competitive JPEG2000 architectures, the encoder chip specifications, under TSMC 0.18 µm CMOS technology are shown in Table 2. The best

evaluation of the proposed encoder vs. other existing works, can be found in performance index value, defined as design throughput per unit area, at 1 MHz. The PI obtained for our core is slightly smaller than indexes of Sanyo [6] and Chang [7] solutions, however none of the competing designs is capable of compressing the signal with a throughput of 180 Msamples/s. This work was also compared to three commercial JPEG2000 encoder products, aimed for HD video broadcast. Results are presented in Table 3 and concern 1080p signal at 4:2:2 sub-sampling. It can be seen that our solution provides the highest frame rate. Additionally proposed encoder core, in contrast to other commercial solutions, supports 1080p30 fps in 4:4:4 signal format. Remarkably is also the fact that at higher bit-rates this core introduces smaller distortions into compressed image than the reference, software encoder. It can be seen in form of R&D curve in Figure 8, obtained for one of the 1920x1080 test images. This situation is particularly visible when number of DWT levels is greater than two and can be explained by rounding error elimination strategies, applied in DWT module.

Table 1 – JPEG2000 encoder implementation results.

Device / Techn.	Xilinx Virtex-5	Altera Stratix III	TSMC 0,18 µm
Area utilization	9360 slices	33150 ALUTs	169 K gates
Memory	1782 KB	830,5 kbits	93 KB (on-chip)
DSP blocks	40	78	-
Max. freq.	110 MHz	125 MHz	125 MHz

Table 2 – JPEG2000 chip comparison in 0,18 µm CMOS process.

Parameter	This work	Sanyo [6]	Chang [7]	Liu [8]
Gate count	179 K	N/A	N/A	180 K
Core area	19 mm2	13 mm2	20,1 mm2	< 20 mm2
Frequency	100 MHz	54 MHz	42 MHz	100 MHz
Power	2 W	0,9 W	384 mW	450 mW
Msamples/s	180	70	124	66
Perf. index	0,095	0,1	0,148	N/A

Table 3 – Commercial JPEG2000 encoder cores comparison.

JPEG 2000 Encoder HD	FPGA device	SDRAM size	Signal	Max. frame rate
This work	xc5vsx95t	64 MB	1080p	45 fps
Barco Silex [9]	xc5vlx110t	96 MB	1080p	30 fps
intoPIX [10]	xc5vlx110t	256 MB	1080p	30 fps
Alma Tech [11]	xc5vlx155t	16 MB	1080p	25 fps

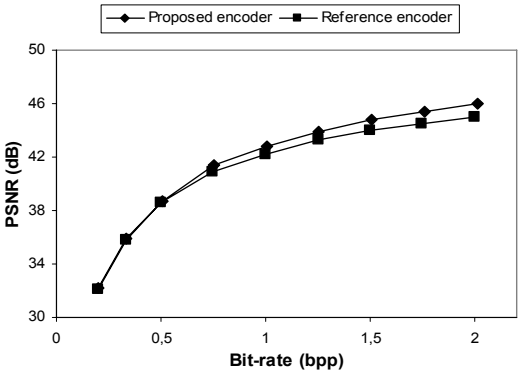

Figure 8 – The proposed encoder codestream quality vs. reference JJ2000 5.1 Java application. Applied encoder settings: two DWT levels, code-block size – 64x64, tile size – 1024x1024.

5. CONCLUSIONS

In the paper we presented a novel, hardware architecture of JPEG2000 encoder, targeted for HD video applications. To meet high-performance requirements of the compression system, an efficient 2-D DWT engine is proposed and integrated in the encoder architecture, together with two parallel channels of EBCOT TIER-1 module. As a result of applied hardware optimizations the maximum throughput of 180 Msamples/s has been achieved for 100 MHz clock and 0.333 bpp compression rate. The proposed encoder core, at competitive area resources, provides superior frame rate and excellent compression quality for HD and Full HD video material. Future works will be focused on constraining power consumption of the design.

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