Optimization of Parallel Processing Intensive Digital Front-End for IEEE 802.11ac Receiver

Juha Yli-Kaakinen, Toni Levanen, Mona Aghababaeetafreshi, Markku Renfors, and Mikko Valkama
Tampere University of Technology, Finland
{juha.yli-kaakinen, toni.levanen, mona.aghababaeetafreshi, markku.renfors, mikko.e.valkama}@tut.fi

***Abstract*—Modern computing platforms offer increasing levels of parallelism for the fast execution of different signal processing tasks. In this paper a digital front-end concept is developed, where the parallel processing is utilized for dividing the inherent structure of IEEE 802.11ac waveform to two or more parallel signals and by processing the resulting signals further e.g, using legacy IEEE 802.11n digital receiver chains. Two multirate channelization architectures are developed with the corresponding filter coefficient optimization. The full radio link performance simulations with commonly adopted indoor WiFi channel profiles are provided, verifying the overall link performance with the proposed channelization architectures.**

I. Introduction

Software-based implementations of radio transceiver digital front-end (DFE) and baseband (BB) processing stages are receiving increasing interest, due to substantially enhanced re-configurability and reduced time-to-market cycles, when compared to classical fixed-function digital hardware implementations [1], [2]. Modern platforms offer increased parallel computational capabilities due to the challenges faced in improving the performance by means of increasing only the clock frequency.

In this paper, we address the DFE processing of the IEEE 802.11ac WLAN/WiFi technology [3], where the basic radio access is based on 80 MHz instantaneous bandwidth. Interestingly, this 80 MHz access waveform is composed by essentially aggregating two 40 MHz sub-signals [3], stemming from the legacy IEEE 802.11n access bandwidth, with three null subcarriers (approximately 1 MHz) inbetween. In the DFE concept proposed in this paper, this overall 80 MHz signal is divided to two 40 MHz sub-signals, through optimized time-domain filtering, which in turn can then be processed forward in parallel, with two smaller-size fast Fourier transforms (FFT) and corresponding frequency-domain processing. This overall receiver principle, assuming also wideband I/Q-downconversion from radio frequency (RF) to baseband, is depicted at conceptual level in Fig. 1. This approach can be extended to a 160 MHz signal to be divided into four 40 MHz signals in a tree structured filter bank configuration.

This filtering task is far from trivial for the following three reasons: First, the cyclic prefix (CP) budget of the overall wireless link, including filtering in the devices, should not be compromised. The frequency selective linear filtering essentially increases the time dispersion introduced by the communication channel and, consequently, increases the interference between the OFDM symbols by reducing the effective CP. Therefore, the channelizer selectivity and the tolerance to time dispersion are two potentially competing requirements. Second, the latency requirements of the IEEE 802.11ac receiver are very tight [3] and particular care has to be taken when considering the potential implementation alternatives for channelizer realization. Third, the small spectral gap of around 1 MHz calls for narrow transition bandwidth in the filter realization and since the FIR filter length is inversely proportional to transition bandwidth its complexity becomes prohibitively high for sharp filters.

For the above mentioned reasons, the channelization filter design task is formulated as an optimization problem in this paper and two alternative channelization architectures are provided with different characteristics and tradeoffs related to latency, filtering performance, and CP budget. First architecture is based on the conventional polyphase halfband filters commonly utilized for sampling rate alternation by a factor of two whereas the second one utilizes non-halfband polyphase filters. However, the main difference between the proposed solutions and the conventional channelization architectures is, that the filtering is carried out using cyclic convolution instead of the linear. Essentially, the cyclic filtering slightly increases the complexity when compared to linear one but this solution does not compromise the CP budget, being implemented after the CP removal. We also provide full radio link simulation results, with commonly adopted WiFi indoor channel models, to verify that the overall channelization filtering does not degrade the link performance.

In the companion paper [4], both C and OpenCL software implementations of the processing with non-cyclic and cyclic halfband filters are described and simulated for comparison purposes on an Intel CPU. Furthermore, the complete software implementation results on the ARM Mali graphic processing unit with half precision floating-point arithmetic are provided in [4].

The rest of the paper is structured as follows. First, in Section II, the channelization architectures based on cyclic multirate filters are introduced and their complexities are discussed. Then in Section III the optimization problem is formulated and a simple design scheme is proposed for designing the initial filter. In Section IV, the comprehensive link performance evaluations are provided to verify and demonstrate that the optimized filtering solutions do not essentially degrade the link performance in any way. Finally, the conclusions are drawn in Section V.

978-0-9928-6265-7/16/$31.00 ©2016 IEEE

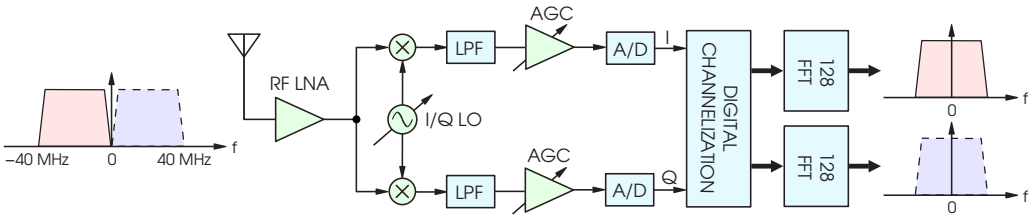

Fig. 1. The overall receiver principle with digital channelization filtering yielding two 40 MHz sub-signals.

II. Channelization Architectures for IEEE 802.11ac

In this work, 80 MHz access bandwidth in IEEE 802.11ac system consisting of 256 subcarriers is considered. 242 subcarriers out of the total 256 are active. Three subcarriers around DC (subcarriers $-1, 0, 1$) are zero and both the negative and positive frequency components contain 121 transmission subcarriers (subcarriers $\pm k$ for $k = 2, 3, \ldots, 122$) [3]. In the IEEE 802.11 standards [5], the total multicarrier symbol duration is defined as 4 µs; 20 percent of this duration (800 ns) is the guard interval which carries the CP of the signal. For FFT size of $L = 256$ this corresponds to the CP of 64 samples.

The goal is to divide the 80 MHz IEEE 802.11ac signal sampled at the Nyquist rate into two 40 MHz-wide signals using linear filtering such that the positive frequency components are separated into one signal and negative frequency components into a second as illustrated in Fig. 1. These are then processed further, in parallel, with two 128-point FFTs and subsequent subcarrier level processing.

The channelization problem stated above can be solved using conventional linear filters before the removal of the CP. The inclusion of the CP effectively converts the linear convolution between the received multicarrier symbols and the channelization filters into the cyclic convolution and thus the passband frequency responses of the channelization filters can be equalized at the subcarrier level after the FFT. However, the linear filter based channelization increases the effective time dispersion of the received signal and, therefore, the filter length and, consequently, the filter performance is limited by the available CP budget.

Alternatively, the channelization can be performed using cyclic filters [6], [7] after the removal of CP without compromising the CP budget as shown in Fig. 2. Let the order of the channelization filter be N and the length of the input data L. The basic idea is to carry out the linear convolution blockwise for the received multicarrier symbols and then cyclically add the last N samples from the resulting $L+N$ samples long sequences to the beginning of the blocks as depicted in Fig. 3. In this case, only the FFT size, the computational complexity, and the latency restrict the order of the channelization filter.

Here, we consider two linear-phase FIR filter structures for realizing the cyclic filters. The first one is based on polyphase halfband filters. These filters are characterized by the property that the number of non-trivial coefficients to be realized for a Nth order filter is $(N+2)/2$. Both the lowpass and highpass

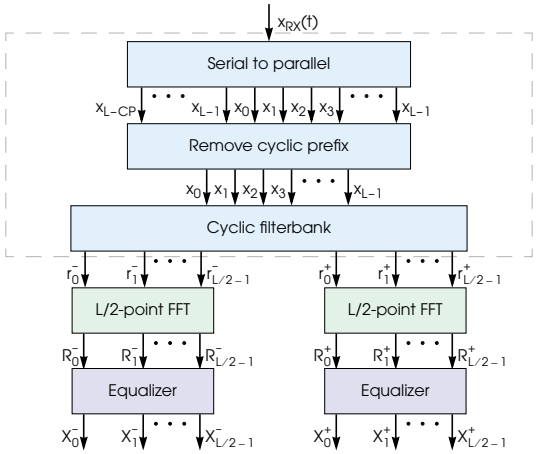

Fig. 2. Channelization architecture based on cyclic filtering.

outputs are obtained at the cost of one additional adder. When the coefficient symmetry is utilized in the linear-phase case, the number of multiplications per real input sample is only $(N+2)/4$. The analytical filter pair, separating the positive and negative frequency components from the complex input signal, is obtained from the halfband filter by multiplying the coefficients h_ℓ of the halfband filter by j^ℓ for $\ell = 0, 1, \ldots, N$. A pair of these filters is required for filtering both the real and imaginary parts of the input signal. The resulting complexity is $C_\mathrm{m} = (N+2)/2$ multiplications per input sample when the coefficient symmetry is utilized [8]. Figs. 4(a) and 4(b) show the magnitude response of the lowpass-highpass halfband and analytical filter pairs, respectively. The active carriers in Fig. 4(b) are denoted by colored area.

The second realization structure is based on polyphase non-halfband filters. In this case, the number of coefficients to be realized is $N+1$. The coefficient symmetry can also be utilized provided that the filters are odd-order linear-phase filters, however two filters are needed for lowpass and highpass filtered outputs and, therefore, the overall number of multiplications per input sample is $N+1$. For the corresponding analytical filter, a pair of filters is needed for filtering the complex input samples resulting to a overall complexity of $C_\mathrm{m} = 2(N+1)$.

The output signals can be decimated by two, if desired, by sharing the input samples into polyphase branch filters such that odd samples go to one branch and even samples to another. In this case, the polyphase branch filters work at the output sample rate, that is, at the half of the input rate and the above

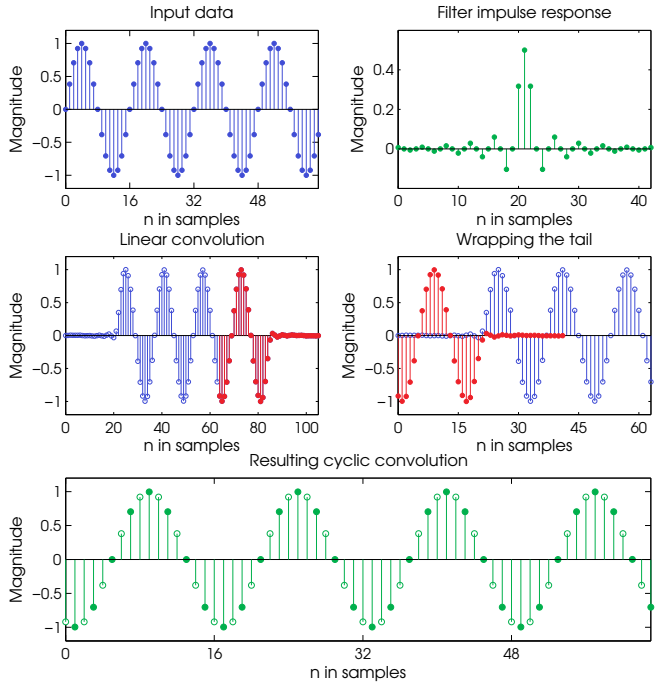

Fig. 3. Illustration of cyclic convolution using linear halfband filter.

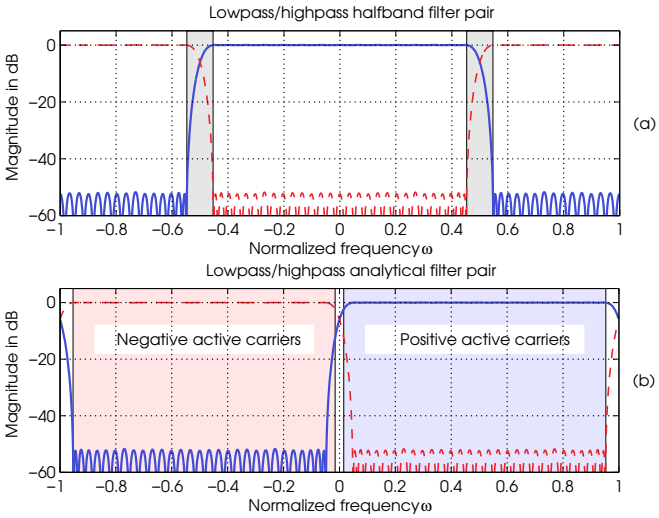

Fig. 4. Magnitude responses of the 58th-order (a) halfband and (b) analytical filter pairs.

complexities can be divided by two.

III. Filter Optimization

In order to optimize the performance of the cyclic filter based channelization architecture, the overall analysis-synthesis filter bank system is decomposed as

$$\mathbf{Y} = \begin{bmatrix} \mathbf{Y}_\mathrm{P} \\ \mathbf{Y}_\mathrm{N} \end{bmatrix} = \begin{bmatrix} \mathbf{H}_\mathrm{P} \\ \mathbf{H}_\mathrm{N} \end{bmatrix} \mathbf{F}_L^{-1}\mathbf{X}. \tag{1}$$

Here, $\mathbf{X}$ is the matrix containing the input symbols on the positive and the negative subcarriers as expressed as

$$\mathbf{X} = \begin{bmatrix} \mathbf{0}_{2\times M} \\ \mathbf{S}_\mathrm{P} \\ \mathbf{0}_{11\times M} \\ \mathbf{S}_\mathrm{N} \\ \mathbf{0}_{1\times M} \end{bmatrix}, \tag{2}$$

whereas the L-by-L inverse DFT matrix $\mathbf{F}_L^{-1}$ represents the synthesis filter bank with L subcarriers. The analysis filter pair can be expressed as

$$\mathbf{H}_\mathrm{P} = \mathrm{diag}(\mathbf{h}_\mathrm{P})\mathbf{F}_{L/2}\mathbf{D}\mathbf{C}_\mathrm{P} \tag{3a}$$
$$\mathbf{H}_\mathrm{N} = \mathrm{diag}(\mathbf{h}_\mathrm{N})\mathbf{F}_{L/2}\mathbf{D}\mathbf{C}_\mathrm{N}, \tag{3b}$$

where $\mathbf{C}_\mathrm{P}$ and $\mathbf{C}_\mathrm{N}$ are the cyclic convolution matrices of the analysis filter pair used for separating the positive and negative subcarriers, respectively. These matrices have the following form

$$\mathbf{C} = \begin{bmatrix} h_0 & 0 & \cdots & 0 & h_N & \cdots & h_1 \\ \vdots & \ddots & \ddots & & \ddots & \ddots & \vdots \\ \vdots & & \ddots & \ddots & & \ddots & \vdots \\ h_N & 0 & & \ddots & \ddots & & 0 \\ 0 & \ddots & & & \ddots & \ddots & \vdots \\ \vdots & \ddots & \ddots & & & \ddots & 0 \\ 0 & \cdots & 0 & h_N & \cdots & \cdots & h_0 \end{bmatrix}, \tag{4}$$

where h_ℓ for $\ell = 0, 1, \ldots, N$ are the impulse response coefficient values of the filter. The $L/2$-by-L downsampling matrix $\mathbf{D}$ is identically an identity matrix with odd-numbered rows removed [9, p. 89]. The frequency responses of the channelization filter pair can be equalized at the passbands of the filters by embedding the inverses of the frequency responses of the channelization filters into the subcarrier-wise equalizer. The embedded equalizer weights on the positive and negative subcarriers are denoted in Eq. (3) by $\mathbf{h}_\mathrm{P}$ and $\mathbf{h}_\mathrm{N}$, respectively. The inclusion and the removal of the CP is not included in the analysis-synthesis pair of Eq. (3) since the channel is assumed to be ideal in the optimization and, therefore, the CP has no effect on the overall performance.

The optimization goal is to minimize the maximum of the root-mean-squared error between the received and transmitted burst of symbols as expressed as

$$\mathbf{e} = \max\|\mathbf{Y} - \mathbf{X}\|_2. \tag{5}$$

Here, the L_2-norm is first evaluated symbols-wise (column-wise) and then the maximum is evaluated subcarrier-wise (row-wise).

In the case, when the frequency responses of the channelization filters have very small magnitude on their passband regions, the embedded equalizer will amplify the received noise on the corresponding subcarriers. Therefore, an additional constraint is needed in the optimization either for constraining (a) the passband ripple of the channelization filters or (b) the

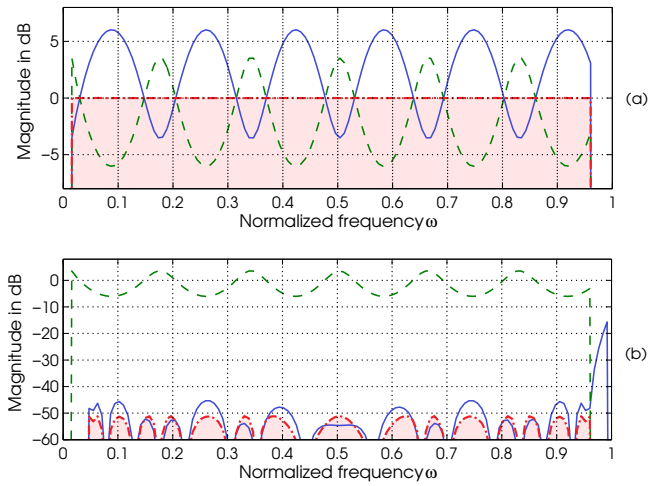

Fig. 5. (a) Magnitude of the positive active carriers on the passband of the analytical filter (solid line), the corresponding equalizer (dashed line), and the magnitude of the filtered and equalized active carriers (dot-dashed line). (b) Magnitude of the aliasing components on the passband of the analytical filter, the corresponding equalizer (dashed line), and the magnitude of the equalized aliasing components (dot-dashed line).

passband ripple of the equalizers. The latter constraint can be expressed as

$$\mathbf{c} = \left|\left|\begin{bmatrix}\mathbf{h}_N & \mathbf{h}_P\end{bmatrix}\right| - 1\right| - \Delta_p, \tag{6}$$

where Δ_p is the desired maximum passband ripple of the equalizers. The resulting optimization problem can be stated as follows: Find the parameters of the channelization filters such that $\mathbf{e}$ is minimized subject to the constraint that $\mathbf{c} \leq 0$. This problem can be solved, e.g., using the `fminimax` function from the MATLAB optimization toolbox.

The initial prototype filter for the optimization can be generated using the Parks-McClellan algorithm as follows: When decimating the resulting lowpass and highpass filtered signals, the residue of the active negative (positive) subcarriers alias above positive (negative) subcarriers, i.e., subcarriers $-k$ for $k = 2,3,\ldots,122$ alias above subcarriers $128-k$ for $k = 2,3,\ldots,122$. Consequently, the stopband edge of the lowpass analytical filter has to be $\omega_s = (128-122)/128\pi = 0.046875\pi$ to prevent aliasing into positive active subcarriers. Correspondingly, the passband and stopband edges of the prototype halfband filter are $\omega_p = 1/2\pi - (128-122)/128\pi = 0.453125\pi$ and $\omega_s = \pi - 0.53125\pi$ as the passband and stopband edges of the prototype halfband filter are located symmetrically around $\pi/2$ as $\omega_s = \pi - \omega_p$ for $\omega_p < \pi/2$ [10]. The gray areas in Fig. 4(a) denote the transition bands of the prototype filter pair.

The magnitude of the aliasing components is defined by the stopband attenuation of the prototype filter. It has been observed that the design with 50 dB attenuation for the aliasing component gives nearly ideal performance in all the simulated cases. Due to the properties of the prototype halfband filters the order of the transfer function is restricted to be $N = 2+4k$, where k is a positive integer [10]. The minimum order of an halfband FIR filter to achieve 50-dB attenuation with passband edge of $\omega_p = 0.453125\pi$ is $N = 58$.

For a non-halfband filter, the order has to be $2k$ in order to utilize the coefficient symmetry in polyphase branches. However, in this case there is a trade-off between the filter order and the passband ripple, that is, for the passband ripple of $\Delta_p = 0.5$ a filter of order $N = 28$ is needed, whereas for $\Delta_p = 0.25$ the filter order has to be increased to $N = 38$. However, as will be shown in next section, the performance of 28th-order filter is sufficient with full-precision floating point arithmetic over a wide range of signal-to-noise ratio values.

The complexity of the 28th-order non-halfband filter in terms of multiplications per sample is approximately double the complexity of the 58th-order halfband filter, however, the latency is only the half. The improved latency properties of the optimized design give increased degrees of freedom for implementing the proposed DFE.

The magnitude response of the optimized 28th-order filter is shown in Fig. 5 using the solid line. The dashed and dash-dotted lines show the magnitude responses of the equalizer and the corresponding combined responses (both analytical filter and equalizer). As can be seen from this figure, the combined response is equal to unity on the passband of the analytical filter and well below -50 dB on the stopband.

IV. Numerical Results

Channel models D and F from [11], [12], have been used to simulate the performance of the proposed two channelization architectures in the case of frequency selective fading channel. These two channel models can be considered to represent the environments with little-to-moderate frequency selectivity, as it is typically the case in indoor typical offices and houses (model D), and moderate-to-large frequency selectivity, common in large indoor spaces such as airports and conference centers (model F).

The symbol error rate (SER) and error vector magnitude (EVM) performances of the channelization architectures have been evaluated in the following cases. In the first case, the performance is evaluated using conventional linear halfband filter where the channelization is carried out before the CP removal [4]. In the second case, the channelization is performed after the CP removal as shown in Fig. 2 either using cyclic halfband filter or cyclic non-halfband filters. In addition, the performance is evaluated in the case with no channelization, that is, the simulation model contains only OFDM-modulator, channel, and demodulator. The minimum stopband attenuation of all the channelization filters is 50 dB. The SER and EVM evaluation is carried out with both the perfect timing synchronization as well as the synchronization error of 8 samples. In all simulations, the number of random channel instances is 1000 whereas the number of 16-QAM OFDM symbols is equal to 100.

The simulated SER and EVM as a function of signal-to-noise ratio (SNR) are shown in Figure 6. As can be seen from this figure, the performance of all the architectures are approximately the same with channel model D. In the case

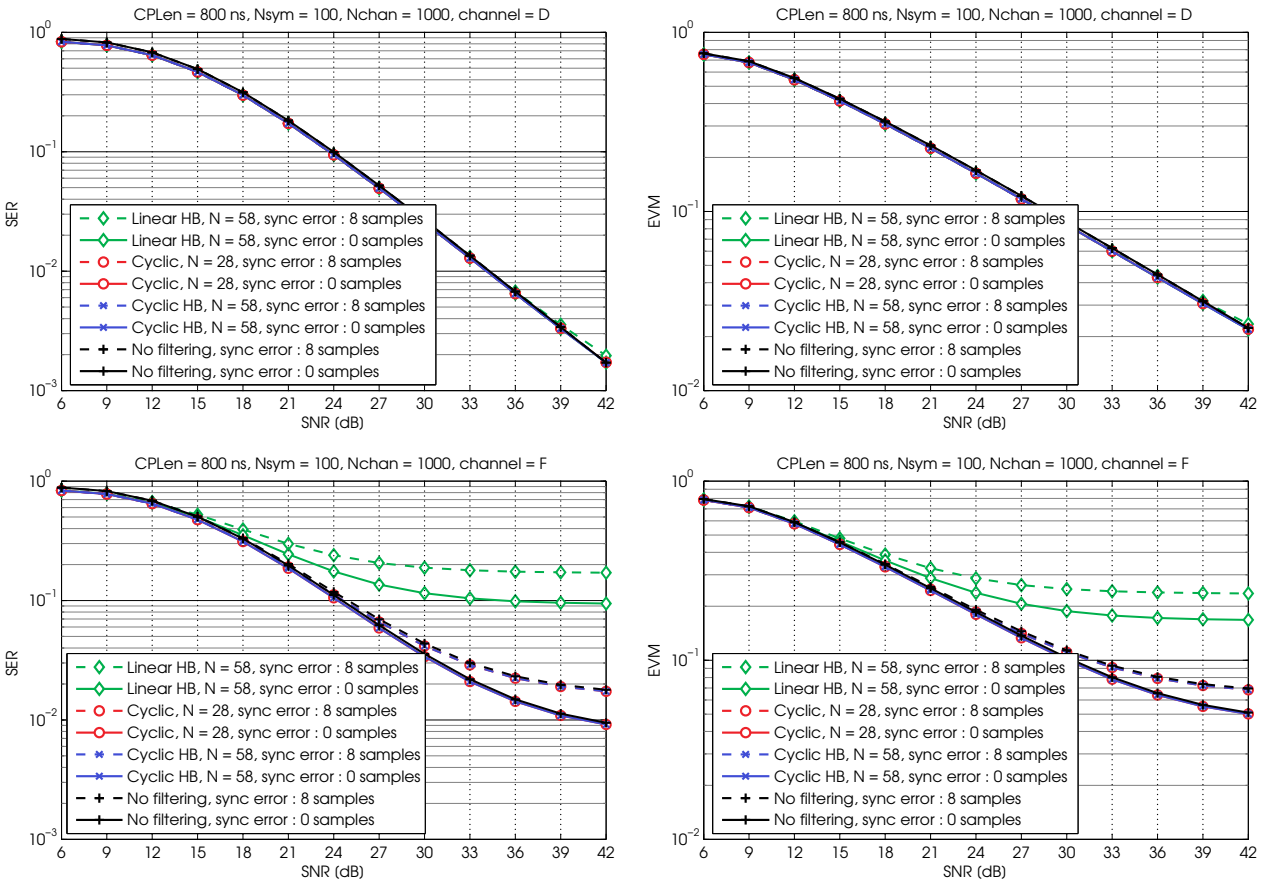

Fig. 6. SER and EVM as a function of SNR for various channelization architectures with channel models D and F.

of channel model F, both the cyclic filter designs result in the considerably better SER and EVM values than linear filter and the performances are the same as with no channelization.

V. Conclusions

In this contribution, two channelization architectures for IEEE 802.11ac waveform are proposed and a design scheme is derived for their optimization. The performance of these architectures is compared using simulations with IEEE WLAN 802.11ac channel models. These simulations show that the channelization architectures based on cyclic convolution provide clearly increased performance when compared to the architecture based on linear filters and the latency as well as the complexity can be traded between the proposed designs without sacrificing the performance.

Acknowledgments

This work was supported by the Finnish Funding Agency for Technology and Innovation (Tekes) under the Parallel Acceleration (ParallaX) project and Nokia Foundation.

References

[1] W. Tuttlebee, Ed., *Software Defined Radio: Baseband Technologies for 3G Handsets and Basestations*. West Sussex: Wiley, 2004.

[2] E. Grayver, *Implementing Software Defined Radio*. New York: Springer, 2013.

[3] *IEEE Standard for Information Technology Telecommunications and Information Exchange Between Systems Local and Metropolitan Area Networks Specific Requirements – Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications – Amendment 4: Enhancements for Very High Throughput for Operation in Bands below 6 GHz*, IEEE Standard 802.11ac-2013, Dec. 2013.

[4] M. AghababaeeTafreshi, J. Yli-Kaakinen, T. Levanen, V. Korhonen, P. Jääskeläinen, M. Renfors, M. Valkama, and J. Takala, "Parallel processing intensive digital front-end for IEEE 802.11ac receiver," in *Proc. Asilomar Conference on Signals, Systems, and Computers*, Nov. 8–11 2015.

[5] *IEEE Standard for Information Technology Telecommunications and Information Exchange Between Systems Local and Metropolitan Area Networks Specific Requirements – Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications*, IEEE Standard 802.11-2012, 2012.

[6] R. Motwani and K. R. Ramakrishnan, "Design of two-channel linear phase orthogonal cyclic filterbanks," *IEEE Signal Processing Lett.*, vol. 5, no. 5, pp. 121–123, May 1998.

[7] P. P. Vaidyanathan and A. Kirac, "Cyclic LTI systems in digital signal processing," *IEEE Trans. Signal Processing*, vol. 47, no. 2, pp. 443–447, Feb. 1999.

[8] T. Saramäki, "Finite impulse response filter design," in *Handbook for Digital Signal Processing*, S. K. Mitra and J. F. Kaiser, Eds. New York: John Wiley and Sons, 1993, ch. 4, pp. 155–277.

[9] G. Strang and T. Nguyen, *Wavelets and filter banks*. SIAM, 1996.

[10] H. W. Schüßler and P. Steffen, "Halfband filters and Hilbert transformers," *Circuits, Syst., Signal Process.*, vol. 17, no. 2, pp. 137–164, 1998.

[11] *TGn Channel Models*, IEEE Standard 802.11-03/940r4, 2004.

[12] *TGac Channel Model Addendum*, IEEE Standard 802.11-09/0308r12, Dec. 2010.