2016 24th European Signal Processing Conference (EUSIPCO)

ParSec: A PSSS Approach to Industrial Radio with Very Low and Very Flexible Cycle Timing

Rolf Kraemer
IHP Microelectronics
Frankfurt (Oder), Germany
kraemer@ihp-microelectronics.com

Michael Methfessel
IHP Microelectronics
Frankfurt (Oder), Germany
methfessel@ihp-microelectronics.com

Rüdiger Kays
Technical University Dortmund
Dortmund, Germany
ruediger.kays@tu-dortmund.de

Lisa Underberg
Technical University Dortmund
Dortmund, Germany
lisa.underberg@tu-dortmund.de

Andreas C. Wolf
Dr. Wolf Wireless GmbH
Teltow, Germany
aw@dw-w.com

***Abstract*—Industry 4.0 is a subject of current relevance which targets detailed information acquisition from industrial production processes. Wireless communication to ease this acquisition process is highly interesting but suffers today from problems of low reliability, high latency and small flexibility. ParSec addresses these subjects by investigating an innovative, CDMA based approach with very low latency of < 50 µs, flexible resource block scheduling and BER of $\leq 10^{-9}$. While the latency figure is completely based on the assumption that a minimum of 3 symbol durations are needed the BER comes from the requirement specification. Two forms of FEC are used to achieve this requested figure. The radio will be used in the frequency range from 5,725 to 5,875 GHz and work without listen before talk. A rapid prototype has been built to conduct channel measurements and prove the promised properties of the PSSS255 approach. The project is conducted in the framework of other "Industrial Radio" oriented projects supported by the German federal ministry of education and research (BMBF).**

Keywords—industrial radio; listen-before talk; PSSS; low-latency; flexible ressource-block allocation

I. INTRODUCTION

Wired and wireless systems have fundamentally different properties in terms of data rate, latency, reliability, and security. This is because the latter uses an error-prone shared medium, which in many cases suffers from difficult channel conditions. Nevertheless, wireless systems are increasingly being deployed in the industrial context, since the flexibility and mobility demanded by modern control systems can only be met in this way. Hereby the requirement of very short latencies in combination with reliability and a high degree of security still poses a major challenge. The classical methods to control the access to the wireless medium do not allow adequate prioritization of data streams due to the necessary "listen before talk" policy. This causes an unpredictable delay before the medium can be accessed. Transmission errors are mainly handled by retransmission.

ParSec [4] investigates and implements a flexible, reliable, and secure wireless communication system which fulfills the requirements of modern industrial automation, i.e. very short latency, high reliability and high security. The basis is an innovative wireless communication procedure which is optimized for "closed-loop" applications and supports latencies of only a few microseconds and delivers a robust resistance against interference. A flexible allocation of resources and a high reliability are guaranteed in complex manufacturing environments. A further focus of the project lies on security issues. In industrial automation, established cryptographic methods are not compatible with the demand for short latencies. For this reason, new approaches for highly efficient encryption/decryption and key management will be investigated. In addition, innovative complementary security techniques will be developed and new ways to generate keys from channel properties and the environment are to be evaluated. In particular, ParSec allows these goals to be reached because the questions of medium access and coding are handled together with the security mechanisms, leading to an overall optimized architecture.

One feature of the project ParSec is the vertical structure, i.e. investigations address all communication layers required by modern automation production, in agreement with the "Industry 4.0" effort. The compatibility with current and future field-bus systems and their firm real-time demands is of central importance and critical for acceptance and marketability of the approach. A significant result of the project is a system demonstrator. It will integrate the innovative wireless communication concept with field-bus based applications as defined by the industrial project partners. This prototypical solution will already employ highly integrated components in order to demonstrate energy efficiency and miniaturization.

One additional aspect of this project is the standardization of ParSec wireless technology. Currently several task-groups are working towards solutions in the 5 GHz ISM band. Special interest is paid to the range from 5.725 to 5.875 GHz. For this spectrum an exclusive permission for use in industrial automation is requested. The permitted emitted power for access without listen before talk should be increased from 14 dBM EIRP [2] to 27 dBm.

“Industrial radio” is an important subject within the German research programs on Industry 4.0. Several research activities are ongoing to improve the use of wireless communication within factories. While for latency values above 1 ms several solutions like WirelessHART [9,10] or WSAN [11,12] are already in place we address systems that require latencies well below 1 ms, demand acceptable error rates and support strong reliability and security concepts. The IEEE 802.15.4 [14] standards group describes several WSN approaches to wireless access in automation systems. One physical access scheme described there is PSSS (Parallel Sequence Spread Spectrum). PSSS as of IEEE802.15.4 supports relatively high data rates in the sub-GHz ISM band of >250 kb/s, has a very good performance in rich scattering environments and shows a very good performance/energy trade-off [5-7].

The remainder of the paper is organized as follows: In Section II we will introduce the target parameters of the anticipated industrial radio system. PSSS basics are introduced in Section III followed by a more detailed mathematical explanation of the signal processing needs in section IV. In section V a short introduction into the required DLC/MAC structures and the concept of flexible resource blocks will be given. Section VI will briefly describe the rapid prototype which is currently available for channel measurements and tests of the new radio system. Section VII will conclude the paper. The project is still in an early stage since it started only in May 2015. Thus, several parameters have to be interpreted as preliminary.

II. TARGET PARAMETERS

Requirement definitions for hard real-time industrial radio systems are given in [13] and [15]. They are derived from existing wired field-bus systems. Please note that we do not address processing delay within our calculations since this is widely application dependent. With our delay figures we therefore set the lower boundary of the achievable delay.

ParSec is based on a new parallel communication strategy which flexibly assigns capacity to the different participants (i.e., nodes) of a closed-loop system transmission in the form of “resource blocks”. This procedure allows extremely short latencies (10 – 100 µs) in combination with high reliability. According to the requirements of the nodes, resource blocks can be configured in several dimensions, leading to optimal performance with minimal use of resources. Radio communication is based on 255-chip parallel spread-spectrum m-sequences, which can be superimposed safely, allowing simultaneous transfer of large number of bits in each symbol [5-8].

Depending on the selected modulation scheme, 255 to 1020 bits can be transferred in every symbol. Client nodes decode and evaluate a subset of the overall bits as determined by their assigned resources. Symbol rates of 200 kHz and higher allow high data rates and extremely short latencies with a required bandwidth of 20 - 50 MHz. It is well known that spread spectrum systems are strongly resistant against narrow-band interference, the typical case in industrial environments. The required frequency bands are available in various ISM bands which lie above 2 GHz. ParSec supports the ETSI initiative TG41 which aims at the assignment of a dedicated band ((5,725 GHz to 5,875 GHz) for closed-loop automation systems. In this range, special means to handle WLAN interference will not be required [1]. The proposed channel spacing and transmit power are fully compatible with the design of the ParSec system.

Table 1: Targets for technical parameters

Parameter	Value	Comment
Medium access method	PSSS255	A variant of CDMA
FEC	0.8...0.95	block codes
Duplex	CDD, FDD,TDD	CDD preferred, TDD as alternative
Bandwidth	20 - 50 MHz	Depends on data rate and modulation
Data rate per node	256 kb/s - 10 Mb/s	Depends on node count and latency requirement
System capacity	50-100 Mb/s	PHY data rate
Range	≤50m	
Packet error rate	$\leq 10^{-9}$	Corresponds to less than 5 errors per year
Symbol rate	200 KHz	Corresponds to 5 µs symbol duration
Modulation	BPSK, 4 PAM 16 PAM	Configurable
Transmit power	0 - 27 dBm	
Acknowledgement	ACK, NACK	Probably not necessary
Encryption	64/80 Bit	Configurable
Nodes per system	10 - 100	Depends on latency/data rate requirements

Furthermore, a code-division duplex (CDD) technique for industry automation is to be investigated and realized for the first time. This full-duplex approach allows a further reduction of the latency and permits an efficient and cost-effective baseband processing. On the other hand, it requires additional intelligent procedures to separate transmit and receive codes [8]. As simpler alternatives, the classic duplex method FDD is also considered in the project. TDD can be used as an alternative if the application accepts higher delays or if we can double the bandwidth and increase the symbol rate by a factor of 2. For acyclic traffic TDD is always an option.

III. PHSICAL LAYER CONCEPT

In contrast to known spread spectrum approaches like DSSS (Direct Sequence Spread Spectrum) that spread each bit with an appropriate spreading code with high auto-correlation value (e.g. Barker 11), PSSS uses m-sequences and all cyclical shifts of the generator sequence. Thus, each code consists of m chips. Generator sequences always have a length of 2^n-1, where n is an integer number. For ParSec we choose n=8 as a compromise between coding effort, bandwidth requirement, throughput and number of independent code channels. With our choice we have 255 channels available. Each PSSS symbol consists of the analog, chip-wise superposition of all chip sequences resulting in a discrete multi-valued amplitude signal that is transmitted via the medium. Each symbol consists of "resource elements" for all 2^n-1 independent channels (Figure 1). A resource element carries between 1 and 4 bits according to the used modulation scheme.

The continuous stream of PSSS symbols will only be interrupted by inserted preambles that are required for synchronization and channel estimation reasons. All other symbols can be used by the MAC layer, collectively forming the usable MAC "resource space" for data and signaling information. Such a system is especially efficient, if the symbol stream is sent without interruption, i.e. in synchronous manner, since the re-synchronization effort at each receiver can be minimized. In ParSec we address both FDD (Frequency Division Duplex) as well as CDD (Code Division Duplex). CDD can be very efficient since we only have to share a single code-space between up-link and down-link information, making the baseband processor quite simple. CDD, however, introduces some additional complications such as the need for frequent power-control and for interference mitigation at client nodes. Both FDD as well as CDD exhibit the advantage of supporting full duplex transmission. This reduces the cycle time and increases the flexibility of resource allocation.

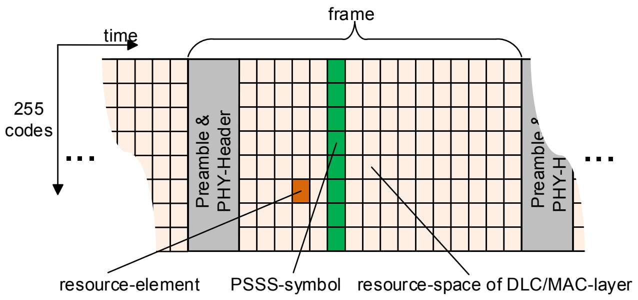

Figure 1: Continuous PSSS Symbol Stream

System bandwidth can be varied by changing the chip rate to allow for increased throughput. Using a bandwidth of 20 MHz we achieve a chip-duration of 50 ns and PSSS symbol duration of 14.25 µs. This assumes a 30 chip cyclic prefix for each symbol to mitigate the effects of inter-symbol interference.

IV. PSSS TECHNOLOGY

A. Basics

Maximum length sequences (m-sequences) are simple to generate by using linear feedback shift registers (LFSR). They are characterized by a polynomial generator.

PSSS uses cyclically shifted m-sequences in parallel. Equation (1) describes the base m-sequence ms_1.

$$ms_1 = \{m_{11}, m_{21}, \dots, m_{M1}) \tag{1}$$

The coding matrix EN is given in (2) and is constructed using (1). The matrix contains cyclically shifted m-sequences based on ms_1

$$EN = \left\{ \begin{matrix} m_{11}\ m_{12} \dots & \dots \dots m_{1N} \\ m_{21}\ m_{22} \dots & \dots \dots m_{2N} \\ m_{M1}\ m_{M2} \dots & \dots \dots m_{MN} \end{matrix} \right\} \tag{2}$$

D is the column vector that represents N data bits as shown in (3). For 1 bit/s/Hz spectral efficiency, N is equal to the length of a m-sequence.

$$D_T = (d_1, d_2, \dots, d_N) \tag{3}$$

For encoding, the data vector D is multiplied with EN resulting in multi-level PSSS symbol vector S as in (4).

$$S = EN \cdot D \tag{4}$$

Since in our realization m-sequences are of length 255, the encoding matrix EN is a [255×255] matrix. Thus, in each PSSS symbol, we encode 255 bits of data.

Decoding of PSSS symbols can be done by cyclic cross correlation of the PSSS symbol vector S with the base m-sequence ms_1. That is, for each m-sequence generated from the base the correlation with S is evaluated individually, resulting in N bits of data. This operation is similar to the multiplication of a decoding matrix 'DE' (as in (5)) with the PSSS symbol vector 'S' resulting in (6).

$$DE = EN^T \tag{5}$$

$$CCF = S \cdot DE \tag{6}$$

CCF is a vector that represents the cyclic correlation between the PSSS symbol S and the decoder matrix DE. The reconstruction of data bits is done by a threshold decision as described in (7)

$$d'_n(ccf_n) = \left\{ \begin{matrix} d'_n = 0;\ \leq (0) \\ d'_n = 1;\ >\ (0) \end{matrix} \right\} \tag{7}$$

Here $d'_n(ccf_n)$ is the reconstructed data bit where a threshold equal to zero has been chosen. Depending on the implementation targets of PSSS, different threshold algorithms can be chosen

B. Channel Deconvolution

We define an effective channel that includes the impairments caused by the physical channel and the RF-frontend electronics. Channel deconvolution is the process by which channel impairments and RF impairments are compensated. Due to the mentioned impairments, the correlation of two cyclic shifted symbols in consecutive positions will suffer from a signal tail that interferes with the original signal in that position. Correcting the channel impairments by proper de-convolution will reduce this effect so that all available codes can be used for transmission.

H shall represent the channel response in the time domain. The PSSS symbol S is convolved with the channel response H resulting in G'. This is the received PSSS symbol as given in (8) where $\tilde{\otimes}$ represents cyclic convolution in the time domain.

$$G' = S \tilde{\otimes} H \tag{8}$$

We write ms_1^{-1} for the time-inverted sequence of (1), used as a correlation reference. CCF' is the cyclic convolution of G' with ms_1^{-1}. CCF' as evaluated in (9) does not compensate for multipath effects and RF impairments.

$$CCF' = G' \tilde{\otimes} ms_1^{-1} \tag{9}$$

H^{-1} is the inverse channel response in the time domain. By convolving it with ms_1^{-1} we obtain $ms_{1\_new}^{-1}$ as new correlation reference as shown in (10).

$$ms_{1\_new}^{-1} = H^{-1} \tilde{\otimes} ms_1^{-1} \tag{10}$$

CCF'_{new} is the cyclic convolution of G' with $ms_{1\_new}^{-1}$ as described in (11). CCF'_{new} as evaluated in (11) compensates for multipath effects and RF impairment losses.

$$CCF'_{new} = G' \tilde{\otimes} ms_{1\_new}^{-1} \tag{11}$$

Thus CCF'_{new} is used in the reconstructions of data bits by threshold decision as described in (7). The calculation of the new decoding reference ms_1^{-1} must be done only when the channel changes, i.e. with a rate greater or equal to the inverse of the channel coherence time.

V. Ressource Management and DLC/MAC Support

If we use FDD or CDD as duplexing method we obtain in both directions a continuous independent resource space for the DLC (Data Link Control) protocols. Resource elements can be arbitrarily placed and grouped. During the design phase of the distribution algorithm, pros and cons of grouping and placements have to be evaluated to achieve a fair trade-off between data transmission and overhead transmission. From the point of view of the automation-systems transmission capacity, signaling data, any protocol control data, data for FEC (Forward Error Correction) or security is considered overhead. Each group of resource elements builds a logical channel between master- and slave nodes.

Control information between the master and slave nodes, e.g. authentication data or protocol negotiation data, must be transmitted additionally. This information is carried in additional logical channels. To avoid a negative impact on latency and cycle time, we decide to send this information not as part of the preamble. This choice allows the flexible resource allocation scheme to be applied to control data as well as user data.

Full duplexing reduces the latency significantly. As lower bound we can assume a latency of only 3 PSSS symbols which results (with our current parameter choices) in a minimal latency of 42.75 µs. This lies well below the requested 1 ms and allows at least 20 nodes to be served simultaneously with this low latency.

Figure 2 shows up- and downlink of an exemplary application with few resource blocks only. It is obvious that up- and downlink are not necessarily symmetric, and that applications with completely different latency requirements can be served simultaneously. This flexibility goes well beyond current field-bus systems which push synchronous frames through transmission pipes. Additionally, nonsynchronous traffic can also be served concurrently, for example for TCP/IP packet-transmissions. From the point of view of the DLC layer we are using a splitted frame. From MAC view non-synchronous data is handled as an ordinary resource block.

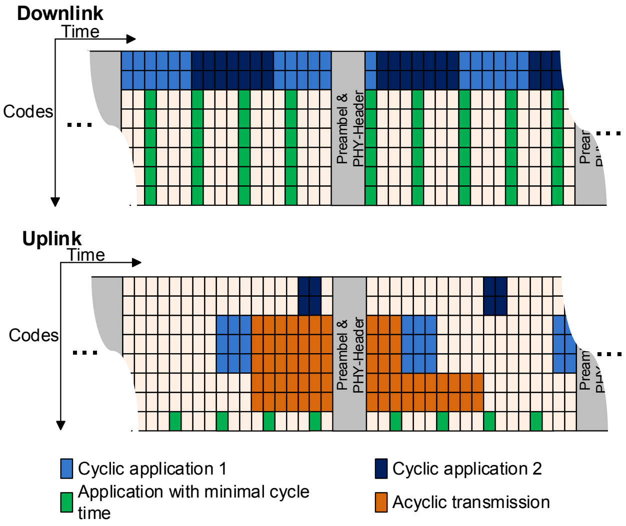

Figure 2: Stream of PSSS symbols with resource blocks.

VI. Rapid Prorotype

To perform early measurements and transmission experiments, the ParSec project developed a rapid prototype. Figure 3 shows the rapid prototype as currently available. It consists of three stacked PCB boards of size 8 x 8 cm. The topmost board is a modified Beaglebone running a Debian Linux operating system. The board is connected to the second board using an 8 bit parallel bus. The second board realizes the PSSS baseband within a FPGA.

The baseband is connected to the third board which is realized by using an “off the shelf“ SDR chip. The application program of the processor board generates bit sequences to be transmitted. The PSSS baseband processor groups the bits into 255 bit wide symbol vectors and transmits them sequentially via the radio interface. All transmit and receive parameters can be controlled and are also accessible. This allows e.g. the access to channel parameters (used in PSSS for deconvolution) to investigate them for use as PUF (physically unclonable function) for node authentication keys.

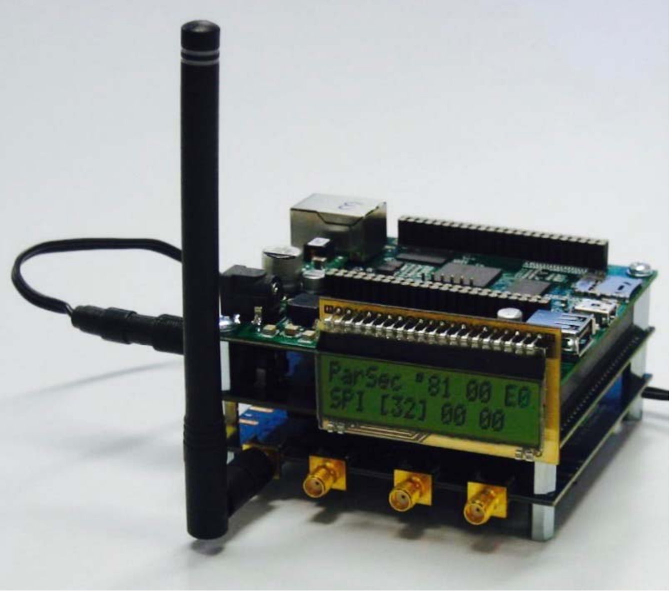

Figure 3: ParSec rapid prototype system

VII. CONCLUSIONS

PSSS is an innovative approach with high potential for industrial radio concepts. Very low latency can be provided within a reasonable bandwidth of only 20 MHz. The performance requirements of automation systems up to 20 Mb/s can be fulfilled. If higher performance is required, chip-rate and thereby bandwidth can be increased. Also the modulation scheme can be modified, trading data rate against SNR requirements. The proper trade-offs for different application scenarios are still under investigation. ParSec has developed a rapid prototype that allows further refinement of systems parameters and more insight into realistic industrial radio channel conditions. We are quite confident that we will be able to contribute with this work to future standardization efforts. In sum, ParSec presents an innovative closed-loop radio system for industrial applications which can deliver low latencies together with a flexible allocation of resources.

ACKNOWLEDGMENT

We would like to thank all ParSec partners. The exact specification is still under development but all partners have contributed to the stabilization process. ParSec is financially supported by the BMBF program "Zuverlässige drahtlose Kommunikation in der Industrie“

REFERENCES

[1] ZVEI: Automation, „Coexistence of Wireless Systems in Automation Technology“, Technical Report, ZVEI - German Electrical and Electronic Manufacturers Association, April 2009

[2] ETSI EN 300 440-1, V1.6.1, Okt. 2010

[3] Wolf, A., "Verfahren zum Übertragen eines Datenwortes; DPMA Offenlegung DE 103 01 250 A1 29.7.2004, Anmeldetag 12.01.2003

[4] BMBF-Project ParSec, www.parsec-projekt.de

[5] Schwetlick, H., Wolf, A.: PSSS - parallel sequence spread spectrum a physical layer for RF communication; Proc. IEEE Int. Consumer Electronics Symp. ; 2004

[6] Wolf, A., Kraemer, R. Scheytt, C.: Ultra-High Speed Wireless Communication with Low Complexity Transceiver; International Symposium on Signal, Systems and Electronics, Potsdam 2012

[7] Wolf, A, Mahlig, M..: Benchmarking of WSN Solutions; Wireless Congress 2010

[8] Mayank J., Jung Il Choiy, Tae Min Kim, Dinesh Bharadia, Siddharth Seth, Kannan Srinivasan, Philip Levis, Sachin Katti, Prasun Sinha: Practical, Real-time, Full Duplex Wireless; MobiCom’11, September 19–23, 2011, Las Vegas, Nevada, USA.

[9] Zhu, Xiuming and Lin, Thomas and Han, Song and Mok, Aloysius and Chen, Deji and Nixon, Mark and Rotvold, Eric: Measuring WirelessHART against wired fieldbus for control; , 10th IEEE International Conference on Industrial Informatics (INDIN), 2012

[10] Abusayeed Saifullah, Chenyang Lu, You Xu, and Yixin Chen: Real-Time Scheduling for WirelessHART Networks; Department of Computer Science & Engineering - Washington University in St. Louis; Campus Box 1045 - St. Louis, MO - 63130 - ph: (314) 935-6160; 2010

[11] PNO: WSAN Air Interface Specification; Technical Specification; Version 1.0; June 2012; Order No.: 2.632

[12] PNO: WSAN System Specification; Technical Specification; Version 1.0; June 2012 Order No.: 2.642

[13] GerlachErhardt, H.: Real Time Requirements in Industrial Automation, PNO TC2/WG12, Oktober 2009

[14] [IEEE-802.15.4]: http://standards.ieee.org/getieee802/download/802.15.4-2011.pdf

[15] Eva Geisberger, Manfred Broy: Integrierte Forschungsagenda Cyber-Physical Systems; acatech STUDIE; März 2012