Energy Harvesting via Analog-to-Digital Conversion

Neha Jain, Nir Shlezinger, Yonina C. Eldar, Anubha Gupta, and Vivek Ashok Bohara

***Abstract*—Analog-to-digital converters (ADCs) allow physical signals to be processed using digital hardware. A common ADC architecture is based on sample-and-hold (S/H) circuits, where the acquired signal is observed in repeated intervals of fixed duration, referred to as the sampling time, and is not utilized for the entire duration. In this paper, we extend the structure of S/H ADCs, allowing them to harvest energy from the observed signal by modifying the circuitry during hold time of the sampling process of an ADC. This harvested energy can be used to supplement the ADC itself, paving the way to the possibility of zero power and power saving ADCs. We analyze the tradeoff between the ability to accurately recover the sampled signal and the energy harvesting which arises from the proposed ADC architecture, and provide guidelines to setting the sampling rate in light of accuracy and energy constraints. Our numerical evaluations indicate that energy harvesting ADCs operating with up to 16 bits per sample can acquire analog signals such that they can be recovered with minimal errors without requiring power from the external source.**

***Index Terms*—Energy harvesting, analog-to-digital conversion.**

I. Introduction

Physical signals are analog in nature, taking values in continuous sets over a continuous time interval. In order to process and extract information from such signals using digital hardware, they must be accurately represented in digital form. Analog-to-digital converters (ADCs) thus play an important role in digital signal processing systems [1]. ADCs are typically a major source of energy consumption, as their power dissipation grows with the sampling rate and the quantization resolution, and thus their ability to accurately represent the acquired signal is typically limited by the available power [2]. Nowadays, ADCs are utilized in a multitude of energy-limited devices, including communication devices [3], wireless sensors [4], and medically implanted devices [5]. Therefore, there is a growing need for ADCs capable of reliably acquiring signals while consuming a low amount of power.

Existing strategies proposed in the literature to facilitate energy efficient acquisition can be divided into those taking a signal processing approach, and techniques focusing on circuit level design. Signal processing methods aim at allowing the ADC to operate at reduced sampling rate and quantization resolution by accounting for how the acquired signal is processed. This is typically achieved by exploiting some a-priori known signal structure which allow recovery from samples of low rate and resolution, as in [4], [6], [7] . Additionally, in scenarios where the signal is acquired for some task, i.e., to recover some underlying information, it was recently shown that the desired information can be accurately recovered from the output of low resolution ADCs by properly designing the acquisition system [8]–[10] . These methods typically focus on the signal model, without accounting for the ADC circuitry.

Circuit level methods design low power ADC hardware without considering the model of the analog signal and the task for which it is acquired. This can be achieved by reducing the circuit power supply [5] and limiting the operating frequency [11], in order to reduce the overall power consumption. An alternative approach is to modify and combine ADC architectures, such as sample-and-hold (S/H) ADCs, flash ADCs, sigma-delta ADCs, and time-interleaved ADCs, to improve their energy efficiency, see, e.g., [12], [13] .

A popular power efficient ADC structure is the S/H based successive approximation register (SAR) architecture, which is capable of operating at high resolution and a small form factor with relatively low power consumption [14]. The power consumption of SAR ADCs can be further reduced by incorporating energy efficient switching schemes, as proposed in [15], [16]. In S/H architectures, the circuit used to sample the input analog signal consists of two phases, *acquisition phase* and *hold phase*. In the acquisition phase, the S/H circuit tracks the input analog signal. The sampled value captured in the acquisition phase is then converted into digital form, i.e., a sequence of bits, during hold phase. Therefore, during the sampling process of S/H ADCs, the input signal is processed only for a small fraction of time (acquisition phase) and neglected/discarded for the remaining time interval (hold phase) [17], [18]. The fact that the signal is not accessed in a dominant portion of the sampling period, motivates the extension of S/H ADCs, and particularly SAR ADCs, to continuously utilize the analog signal in order to mitigate power consumption.

In this work we combine circuit level methods with signal processing tools to improve the energy efficiency of S/H ADCs by allowing them to *harvest energy* from the acquired signal. We introduce an additional energy harvesting circuit, building upon our previous works [19], [20], which demonstrated the hardware feasibility of combining energy harvesting and analog-to-digital conversion. In the resulting architecture, referred to as *eSampling*, the signal is harvested during hold phase, i.e., when it is not utilized in conventional S/H ADCs.

By modeling the input signal as a stationary process, we analyze the tradeoff between the ability to accurately reconstruct the signal from its samples and the energy harvested from it. Our analysis identifies how to set the sampling rate to optimize this tradeoff when operating under energy constraints or fidelity restrictions on the reconstruction. As a special case, we characterize the maximal accuracy in which a signal can be eSampled using only harvested energy, i.e., without requiring any energy from its power source. We numerically demonstrate that eSampling SAR ADCs are capable of reconstructing a broad range of analog signals with minimal distortion while harvesting at least as much energy as they consume.

The rest of this paper is organized as follows: In Section II

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we present our the eSampling system model. Section III analyzes the associated energy-fidelity tradeoff. Section IV details numerical evaluation of the eSampling ADC.

II. System Model

In this section we detail the proposed ADC model. We begin by briefly reviewing S/H-based SAR ADCs and their associated energy consumption in Subsection II-A. Then, we present how SAR ADCs can be extended into *e*Sampling ADCs which harvest energy in addition to signal acquisition in Section II-B. Finally, we formulate the problem of analyzing *e*Sampling ADCs and their associated fidelty-energy tradeoff in Subsection II-C.

A. Sample-and-Hold ADC Model

S/H is a common ADC architecture. Such ADCs acquire each sample in two phases, determined by a switch S as illustrated in Fig. 1: In acquisition phase, the signal is connected to a capacitor referred to as a holding capacitor, $C_{\rm h}$, which is charged to the input analog voltage, as depicted in Fig. 1(a). The time required by $C_{\rm h}$ to charge to the input voltage, which dictates the acquisition time, is given by [14]

$$T_{\rm aq} = \alpha_\tau R_{\rm on} C_{\rm h}, \tag{1}$$

where $R_{\rm on}$ is the on-resistance of the switch S and α_τ time constants is required for the capacitor to be fully charged. Once the acquisition phase is over, the hold phase begins, in which the discrete sample, i.e., the voltage stored in the holding capacitor, is quantized into digital bits. During hold phase, whose duration is denoted by $T_{\rm h}$, the input signal is disconnected from the S/H circuit and $C_{\rm h}$ holds the acquired voltage to accomplish the successful conversion of the acquired sample into digital bits as illustrated in Fig. 1(b). Both $T_{\rm h}$ and $C_{\rm h}$, must be set to allow the quantization circuit of the ADC to complete the conversion.

When the quantizer is based on SAR logic, the overall architecture is referred to as a SAR ADC. An n-bit SAR ADC consists of a comparator, digital-to-analog converter (DAC), and an SAR logical circuit which successively refines the digital representation. To allow successful quantization into n bits, $C_{\rm h} = 2^n C_{\rm u}$, where $C_{\rm u}$ is the unit capacitor of the DAC array used in SAR ADC [17]. The hold time required to quantize each sample must satisfy [18]

$$T_{\rm h} \geq n\alpha_\tau R C_{\rm h}, \tag{2}$$

where R is the equivalent resistance of binary scale switches, i.e., a fixed parameter of the quantization circuit. Therefore, the sampling period, i.e., the duration of acquiring a single sample, is lower bounded by following expression

$$T_{\rm s} = T_{\rm aq} + T_{\rm h} \geq (R_{\rm on} + nR)\alpha_\tau C_{\rm h}. \tag{3}$$

During acquisition phase, the main source of energy consumption is that used by the switch S, which equals

$$E_{\rm aq} = V_{\rm ref_1} \int_0^{T_{\rm aq}} I_{\rm aq}(t) dt, \tag{4}$$

where $V_{\rm ref_1}$ is the power supply and $I_{\rm aq}(t)$ is the current drawn at time instance t. The energy consumption during hold phase can be decomposed in the energy used by each of the components taking part in the quantization procedure. Consequently, the energy consumption during hold phase is $E_{\rm hold} = E_{\rm DAC} + E_{\rm c} + E_{\rm sl}$, where $E_{\rm DAC}$, $E_{\rm c}$, and $E_{\rm sl}$ are the energy consumption of DAC array, comparator, and SAR logic, respectively, per sample. Let $V_{\rm ref_2}$ be the voltage of the quantizer power supply, which has to be larger than the input magnitude with high probability in order to avoid overloading [8]. The energy consumed by the DAC array can be expressed as [17]

$$E_{\rm DAC} = \sum_{i=1}^{n} 2^{n+1-2i}(2^i - 1) C_{\rm u} V_{\rm ref_2}^2 \overset{(a)}{=} \beta_{\rm n} \frac{T_{\rm aq}}{\alpha_\tau R_{\rm on}} V_{\rm ref_2}^2, \tag{5}$$

where (a) follows from the setting of $C_{\rm h} = 2^n C_u$ and (1) by defining $\beta_{\rm n} := \frac{2}{3}(2 - 2^{-n}(3 - 2^{-n}))$. Further, the energy consumption of a dynamic latch comparator used in the SAR ADCs is given by $E_{\rm c} = nC_1 V_{\rm ref_2}^2 + 2V_{\rm ref_2}\gamma_{\rm n}$ [21], where $\gamma_{\rm n} := V_e C_1 \left(n \ln 1/A_k + \frac{n(n+1)}{2} \ln 2 + n \right)$, and C_1, A_k and V_e are the design parameters. The SAR logic is typically implemented using $2n$ D flip-flop circuits, and the energy consumption is given by $E_{\rm sl} = 16n^2 g C_2 V_{\rm ref_2}^2$ [21], where where C_2 is the input capacitance of minimum sized inverter used to design D flip-flop in SAR logic and $0 \leq g \leq 1$ is the total activity of the SAR logic. This implies the energy consumption during hold phase is

$$E_{\rm hold} = V_{\rm ref_2}^2 \left(\beta_{\rm n} \frac{T_{\rm aq}}{\alpha_\tau R_{\rm on}} + nC_1 + 16n^2 C_2 g \right) + 2V_{\rm ref_2}\gamma_{\rm n}. \tag{6}$$

From (1) and (2), we note that for relatively high resolution quantizers, e.g., $n \geq 8$, it holds that $T_{\rm h} >> T_{\rm aq}$, as $T_{\rm h}$ grows with the number of bits per sample [18]. The energy consumption is typically a function of the time duration and the amount of power drawn from the supply, which are negligible in acquisition phase, while comparing to the hold time [15], [18]. Therefore, S/H ADCs consume significantly more energy during hold phase (6) compared to acquisition phase (4). In particular, $E_{\rm hold}$ grows dramatically with n, which makes energy consumption a major bottleneck of high resolution ADCs, motivating the proposed *e*Sampling architecture detailed next.

B. eSampling ADC Architecture

As mentioned above, during hold phase, $C_{\rm h}$ holds the acquired voltage sample, which is converted into a set of digital bits. During this interval, the input signal is disconnected from the circuit by the switch S. In order to mitigate the energy consumption of S/H SAR ADCs without modifying their sampling and quantization procedure, we propose to harvest the input signal energy by connecting it to an energy harvesting circuit during the hold phase, as illustrated in Fig. 2. The proposed architecture, referred to as *e*Sampling ADC, is based on our previous work [19], [20], which demonstrated the hardware feasibility of harvesting energy during acquisition.

The energy harvesting circuit is designed by using passive elements such as rectifier and storage capacitor/supercapacitor

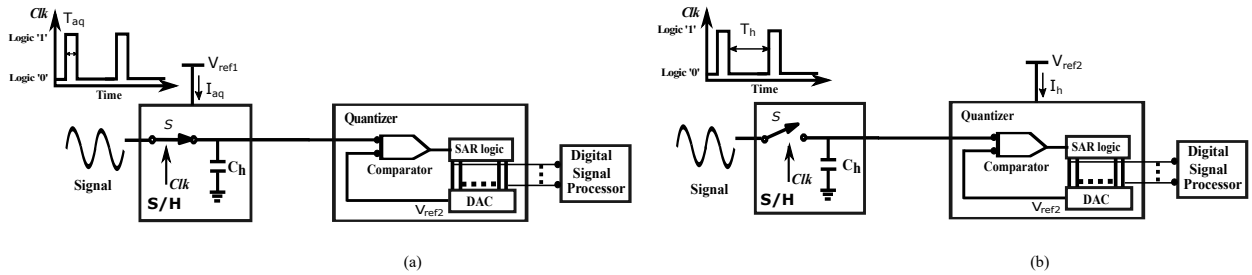

Figure 1. S/H SAR ADC illustration: (a) acquisition phase (b) hold phase

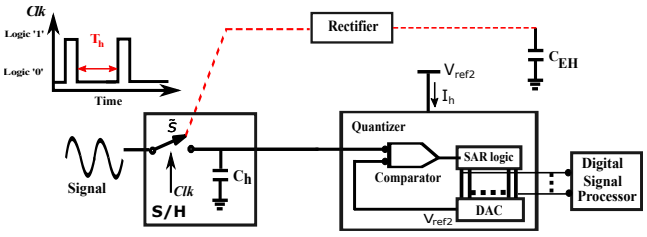

Figure 2. Proposed energy harvesting phase (modified hold phase)

(C_{EH}), and hence no external power supply is required [22] . The rectifier converts the signal into direct current, facilitating its storage in C_{EH}. In order to connect the input signal to the quantization circuit during acquisition time and to the energy harvesting circuit during hold time, the sampling switch S is replaced by a dual switch $\tilde{S}$. The dual switch can be operated with the same clock pulse, by implementing one switch using an NMOS circuit and another using a PMOS circuit, as done in [19]. Both switches are operated with the same clock pulse, and hence no extra power source is required.

The amount of time during which energy is harvested from the input signal per sampling period is at most the hold time $T_{\rm h}$. Recalling $T_h >> T_{aq}$, a significant amount of time can be allocated for harvesting energy from the input signal. The problem of tuning the ADC parameters accounting for the need to acquire the signal and harvest its energy is formulated next.

C. Problem Formulation

The *e*Sampling ADC detailed above harvests energy during hold phase. This implies that more energy can be harvested by increasing the hold time, which in turn increases the sampling period, potentially degrading the ability to reconstruct the signal from its samples. We therefore wish to analyze the fundamental tradeoff between the amount of energy harvested in eSampling and the resulting fidelity in signal reconstruction.

To that aim, we consider a stochastic input signal $x(t)$ modeled as a zero-mean wide sense stationary (WSS) process, variance σ_x^2, and power spectral density (PSD) $S_x(f)$. The signal $x(t)$ is sampled uniformly at rate denoted $T_{\rm s}$, resulting in the discrete-time signal $x(nT_{\rm s})$, which is quantized with n bits per sample into the digital sequence $\tilde{x}(nT_{\rm s})$. The digital representation is used to reconstruct the analog signal $x(t)$ using a linear reconstruction filter. The reconstructed signal with filter $G(t)$ is $\hat{x}(t) = \sum_{k\in\mathcal{Z}} G(t-kT_{\rm s})\tilde{x}(kT_{\rm s})$. The overall system is illustrated in Fig. 3.

The normalized mean square error (NMSE) in reconstructing $x(t)$ is given by $\zeta = \frac{1}{\sigma_x^2 T_{\rm s}} \int_0^{T_{\rm s}} \mathbb{E}\{|x(t)-\hat{x}(t)|^2\}dt$, where $\mathbb{E}\{\cdot\}$ is the stochastic expectation. The amount of expected energy harvested per sampling period is given by

$$E_h = \eta \int_{T_{\rm aq}}^{T_{\rm s}} \mathbb{E}|x(t)|^2 dt = \eta T_{\rm h} \sigma_x^2, \tag{7}$$

where η is the efficiency of the energy harvesting circuit. As mentioned above, the energy harvesting circuit is comprised of passive elements, and does not require an external power source. Therefore, the amount of overall energy consumption per sample using proposed eSampling ADC is given by $E_{\rm aq} + E_{\rm hold} - E_{\rm h}$ as illustrated in Fig. 3. The ratio of the amount of energy harvested to the energy consumption per sample is $E_{\rm ratio} = \frac{E_{\rm h}}{E_{\rm aq}+E_{\rm hold}}$. The value of $V_{\rm ref_2}$ can be written as some multiple $K > 1$ of the input standard deviation, i.e., $V_{\rm ref_2} = K\sigma_x$. This general formulation allows us to relate the reference voltage with the overload probability of the quantizer, $P(|x(t)| \geq V_{\rm ref_2}) \leq K^{-2}$ by Chebyshev's inequality [8]. Further, recalling $E_{\rm aq} << E_{\rm hold}$, $E_{\rm ratio}$ follows from (6) and (7) that

$$E_{\rm ratio} = \frac{\eta(T_{\rm s}-T_{\rm aq})\sigma_x^2}{\left(\frac{\beta_{\rm n} T_{\rm aq}}{\alpha_\tau R_{\rm on}} + nC_1 + 16n^2 C_2 g\right) K^2\sigma_x^2 + 2\gamma_{\rm n} K\sqrt{\sigma_x^2}}. \tag{8}$$

In this paper, we aim to characterize the fundamental tradeoff between the reconstruction accuracy, modelled as the NMSE, and the portion of energy consumed in analog-to-digital conversion harvested by eSampling, referred to as the *energy-fidelty tradeoff*. To trade energy efficiency for fidelity, we modify the sampling rate for a fixed quantization resolution n and fixed acquisition time $T_{\rm aq}$: By increasing the sampling rate the reconstruction accuracy is improved, while the *e*Sampling ADC can harvest less energy, hence the inherent tradeoff between these parameters. In particular, we focus on ADCs operating with relatively high quantization resolution, n, where energy consumption constitutes a major challenge. The following analysis sheds light on the potential of joint acquisition and energy harvesting. For example, it quantifies the minimal recovery NMSE which allows a fixed n-bit ADC to operate at zero power, i.e., $E_{\rm ratio} = 0$ dB. Alternatively, it identifies the n for the ADC can sample a bandlimited signal at Nyquist rate and operate at zero power.

III. *e*Sampling ADC Analysis

In this section, we characterize the energy-fidelity tradeoff which arises from the *e*Sampling ADC paradigm. To that aim, we first derive the recovery NMSE in Subsection III-A. We then formulate and discuss the energy-fidelity tradeoff in Subsections III-B-III-C, respectively.

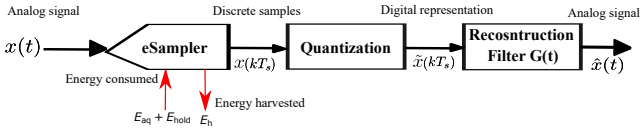

Figure 3. Acquisition in reconstruction via eSampling ADC illustration.

A. Reconstruction NMSE

In general, the NMSE depends on both the sampling rate as well as the quantization resolution [23]. Since we focus on relatively high rate quantization, the NMSE due to quantization is well approximated by the 6 dB rule-of-thumb and is thus of order of $10^{-0.6n}$ [14], resulting in a negligible contribution to the overall NMSE, less than roughly 10^{-5} for $n \geq 8$. Therefore, we henceforth focus on the NMSE between $x(t)$ and $\hat{x}(t)$ due to the sampling procedure, expressed in the following theorem, derived in [7] :

***Theorem** 1:* The minimal achievable NMSE in reconstructing a uniformly sampled WSS signal $x(t)$ with sampling frequency $f_s = 1/T_\mathrm{s}$ using linear reconstruction filter, $G(t)$ is

$$\zeta(T_\mathrm{s}) = 1 - \frac{1}{\sigma_x^2}\sum_{k\in\mathcal{Z}}\int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} \frac{|S_x(f-kf_s)|^2}{\sum_{k'\in\mathcal{Z}} S_x(f-k'f_s)}df. \quad (9)$$

Theorem 1 generalizes the celebrated Shannon-Nyquist theorem, as shown in [7]. The results above provide a characterization of the achievable NMSE, which is used in the sequel to analyze the fidelity-energy tradeoff in eSampling.

B. Energy-Fidelity Tradeoff

Using the expressions for the achievable NMSE (9) and the ratio between energy harvested and consumption (8), we next characterize the energy-fidelity tradeoff of eSampling. We assume that the electromagnetic properties of the circuit components are given, and fix the quantization resolution n in our analysis. Under this setting, T_aq is fixed by (1), and the main design parameter is the hold time T_h, or equivalently, the sampling period T_s. The energy-fidelity tradeoff of eSampling is thus encapsulated in two complementary optimization problems: The first aims at finding the minimal achievable NMSE under a given energy constraint $\delta > 0$, i.e.,

$$\zeta^\mathrm{o}(\delta) = \min_{T_\mathrm{s}>T_\mathrm{aq}} \zeta \qquad \text{s.t. } E_\mathrm{ratio} \geq \delta. \quad (10)$$

For instance, setting $\delta = 0$ dB, implies $E_\mathrm{aq}+E_\mathrm{hold} = E_\mathrm{h}$, this will reveal the minimal NMSE when operating at zero power. A positive value of δ (in dB) implies an energy saving ADC which harvests more energy than its consumption per sample.

An alternative formulation seeks to maximize the energy harvested under a given fidelity constraint $\epsilon > 0$, i.e.,

$$E^\mathrm{o}_\mathrm{ratio}(\epsilon) = \max_{T_\mathrm{s}>T_\mathrm{aq}} E_\mathrm{ratio} \qquad \text{s.t. } \zeta \leq \epsilon. \quad (11)$$

For example, $E^\mathrm{opt}_\mathrm{ratio}(0)$ represents the maximal portion of the consumed energy which can be harvested when seeking ideal recovery, e.g., Nyquist rate sampling for bandlimited $x(t)$.

Problems (10)-(11) allow to characterize the energy-fidelity tradeoff, stated in the following theorem:

***Theorem** 2:* Let $T_\mathrm{h}(\delta)$ be given by

$$T_\mathrm{h}(\delta) := \frac{\delta K^2}{\eta}\left(\frac{\beta_\mathrm{n}T_\mathrm{aq}}{\alpha_\tau R_\mathrm{on}} + nC_1 + 16n^2C_2 g\right) + 2\gamma_\mathrm{n}K\frac{\delta}{\eta\sqrt{\sigma_x^2}}.$$

By setting $f_s(\delta) = \frac{1}{T_{aq}+T_\mathrm{h}(\delta)}$, the solution to (10) is

$$\zeta^\mathrm{o}(\delta) = 1 - \frac{1}{\sigma_x^2}\sum_{k\in\mathcal{Z}}\int_{-\frac{f_s(\delta)}{2}}^{\frac{f_s(\delta)}{2}} \frac{|S_x(f-kf_s(\delta))|^2}{\sum_{k'\in\mathcal{Z}} S_x^H(f-k'f_s(\delta))}df. \quad (12a)$$

Similarly, by letting $T_\mathrm{s}(\epsilon)$ be the maximal sampling interval satisfying $\zeta(T_\mathrm{s}(\epsilon)) = \epsilon$ in (9), then the solution to (11) is

$$E^\mathrm{o}_\mathrm{ratio}(\epsilon) = \frac{\eta(T_\mathrm{s}(\epsilon) - T_\mathrm{aq})\sigma_x^2}{\left(\frac{\beta_\mathrm{n}T_\mathrm{aq}}{\alpha_\tau R_\mathrm{on}} + nC_1 + 16n^2C_2 g\right)K^2\sigma_x^2 + 2\gamma_\mathrm{n}K\sigma_x}. \quad (12b)$$

Proof: The theorem follows by noting that $\zeta(T_\mathrm{s})$ (9) is monotonically decreasing in T_s, while E_ratio in (8) is a monotonically increasing function of T_s. Consequently, both (10) and (11) are obtained by identifying the minimal/maximal value of T_s for which the constraint holds with equality. ■

C. Discussion

The characterization of the energy-fidelity tradeoff in Theorem 2 identifies the achievable energy ratio for a given recovery accuracy and vice versa. The fundamental balance between these measures follows from the structure of *e*Sampling ADCs, in which increasing the hold time degrades the ability recover the signal from its samples, while allowing to harvest more energy. This unique property of *e*Sampling can in fact lead to ADCs which harvest more power than they consume, as numerically demonstrated in Section IV.

The S/H-based SAR ADC model used in our analysis is based on the conventional SAR ADC architecture [21]. The energy-fidelity tradeoff can be further improved by considering more power efficient variations of SAR ADCs, such as the merge capacitor switching based SAR ADC designed in [15], which reduces E_DAC in (5) by 93.4%. Moreover, our characterization considers the general family of stationary signals. When the signal obeys some structure, e.g., it is known to reside in a shift-invariant space, ideal recovery can be achieved at low sampling rates using generalized sampling methods [1], allowing to harvest more energy without affecting the recovery NMSE. We leave the analysis of *e*Sampling of structured signals for future work.

IV. Numerical Analysis

In this section we numerically evaluate the energy-fidelity tradeoff of eSampling ADCs, characterized in Theorem 2, for various ADC configurations. We consider two models for the analog input signals with the following PSDs:

- *Unimodal PSD*: $S_x(f) = \alpha e^{-\frac{f^2}{2\sigma^2}}$, where $\alpha = \frac{\sigma_x^2}{\sqrt{2\pi\sigma^2}}$ such that $\int_{-\infty}^{\infty} S_x(f)df = \sigma_x^2$. The parameter σ^2 controls the PSD width, and the signal is approximately bandlimited with frequency $f_m = 3\sigma$. The considered value of f_m and σ_x^2 are 50 MHz and 1 μW, respectively.
- *Multimodal PSD*: $S_x(f) = \frac{\alpha}{2}(e^{-\frac{(f+f_t)^2}{2\sigma^2}} + e^{-\frac{(f-f_t)^2}{2\sigma^2}})$, where $f_t = 12.5$ MHz. The resulting signal is approximately bandlimited $f_m = 6\sigma$, which we again fix to 50 MHz to be consistent with unimodal setup.

We set $K = 10$, guaranteeing a probability of over 99% that $|x(t)| \leq V_{\mathrm{ref}_2}$, and hence the ADC accuracy is not

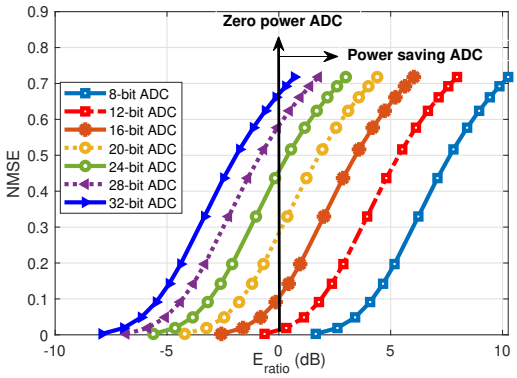

Figure 4. NMSE (ζ) versus E_{ratio}, unimodal PSD.

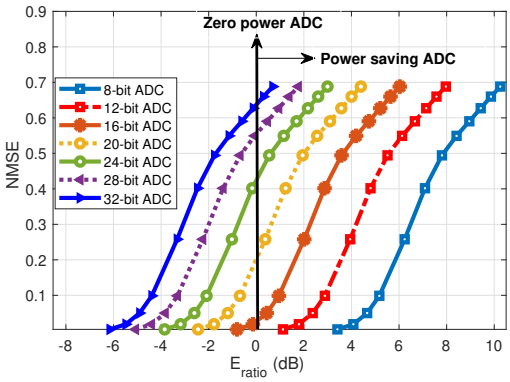

Figure 5. NMSE (ζ) versus E_{ratio}, multimodal PSD.

compromised by quantizer overloading. The remaining system parameters are set following [21], [24] to $\alpha_\tau = 5$, $T_{\text{aq}} = 2$ ns, $R_{\text{on}} = 40\ \Omega$, $A_k = 1.8$, $V_e = 0.1$ V, $C_1 = C_2 = 20$ fF and $g = 0.4$. Finally, we set the efficiency of the energy harvesting system η to be 60%. Figs. 4 and 5 depict the resulting energy-fidelity tradeoff, i.e., the NMSE against the E_{ratio} (in dB) by varying the sampling rate, for unimodal and multimodal PSD, respectively. The results demonstrate that *e*Sampling ADCs can operate with zero power while achieving approximately ideal reconstruction when using up to $n = 12$ and $n = 16$ bit for inputs with unimodal and multimodal PSDs, respectively. Furthermore, it is also observed that *e*Sampling ADCs operating with less than 16 bits are capable of saving power. However, this mode of operation comes at the cost of increased NMSE for higher values of n. For instance, NMSE values of around 0.1 and 0.2 are obtained for $n = 16$ and $n = 20$ bit, respectively, with $E_{\text{ratio}} = 0$ for inputs with unimodal PSD. The numerical results indicate that the power consumption of high resolution ADCs can be notably reduced and even mitigated by properly combining acquisition and energy harvesting via *e*Sampling.

V. Conclusion

In this paper, we proposed the *e*Sampling ADC architecture, which modifies the traditional sampling process of a S/H ADC to harvest energy from the discarded portion of the input signal. We analyzed the amount of energy which can be harvested from stationary signals, and characterized the underlying fundamental tradeoff between energy harvested and reconstruction fidelity which arises from the joint acquisition and energy harvesting paradigm. Our numerical results demonstrate the potential of *e*Sampling in realizing ADCs operating with high resolution and near ideal reconstruction accuracy while harvesting an amount of energy which approaches and can surpass that consumed in acquisition, indicating its potential in realizing self-powered ADCs.

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