Compressive Digital Receiver:
First Results on Sensitivity, Dynamic Range and Instantaneous Bandwidth Measurements

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Abstract—In this work, sensitivity, one/two-signal dynamic range and instantaneous bandwidth measurement results of the recently developed Compressive Digital Receiver (CDR) hardware for Electronic Support Measures (ESM) applications, will be reported for the first time. Developed CDR is a compressive sensing based sub-Nyquist sampling receiver, which can monitor 2.25 GHz bandwidth instantaneously by using four ADCs (Analog-to-Digital Receiver) each of which has a sampling rate of 250 MHz. All the digital processing blocks of the CDR are implemented in Field Programmable Gate Array (FPGA) and they work in real time. It is observed that the sensitivity and dynamic range of the CDR changes with respect to input signal frequency. For 2.25 GHz bandwidth, the best and worst sensitivity values of the CDR are reported as -62 dBm and -41 dBm, respectively. One-signal dynamic range of CDR is measured as at least 60 dB for the whole band. The best and worst values of the two-signal dynamic rage values are observed as 42 dB and 20 dB, respectively.

Index Terms—compressive sensing, digital receiver, sub-Nyquist sampling, sensitivity, one/two-signal dynamic range, instantaneous bandwidth.

I. INTRODUCTION

With the recent developments in radar technology, the requirements of ESM systems have become harder. One of the most important requirements of an ESM system is the instantaneous bandwidth of its digital receiver [1]. In traditional digital ESM receivers, the sampling rate of the ADC used defines its instantaneous bandwidth. In today's most advanced ESM systems, ADC's with sampling rate up to 3 GHz are used. Although this rate enables achieving an instantaneous bandwidth of 1.5 GHz in theory, in practical implementations at most 1 GHz bandwidth is obtained. Also, as the sampling rate of ADCs increase, their dynamic range (number of bits) decrease. Note that an ESM system typically requires at least 30 dB instantaneous dynamic range, which corresponds to at least 8 bit representation levels for the ADCs. Hence, new digital receiver technologies should be developed to achieve higher instantaneous bandwidths (>2 GHz) with lower sampling rates based on sub-Nyquist sampling methods.

One of the most important sub-Nyquist sampling methodologies is compressive sensing based architectures. In literature, many methods have been proposed for compressive sampling based sub-Nyquist sampling [2]–[4]. In all of these methods, although the proposed theory is very fluent and straight forward, no real data results have been shared. In [5], design of an RF (Radio Frequency) circuitry for implementing the analog compression method in [4] is detailed. However, implementation details of the recovery algorithm on a real hardware together with the real data results are omitted.

In this work, sensitivity, one/two-signal dynamic range and instantaneous bandwidth measurement results of the recently developed CDR hardware, which detects the radar pulses and measures their parameters such as TOA (time of arrival), PW (Pulse Width), amplitude, frequency etc., will be reported for the first time. The developed hardware is based on the MWC (Modulated Wideband Converter) technique given in [4], however has a totally original RF and digital hardware design. Preliminary offline recovery results on real data acquired by the prototype hardware has been given in [6]. In this work, sensitivity, one/two-signal dynamic range and instantaneous bandwidth measurement results of the final hardware design will be shared.

CDR is mainly composed of two blocks: i)Analog Processing Block and ii) Digital Processing Block. In the Analog Processing Block, incoming RF signal is compressed in the spectrum by using analog circuits. In the Digital Processing Block, the low bandwidth, compressed data is digitized by using four ADCs each of which sampling at 250 MHz rate. The recovery algorithm, OMP (Orthogonal Matching Pursuit), is utilized over the collected samples, where the total data rate is 1GHz. The Digital Processing Block has been fully implemented in FPGA and is running in real time. Conducted experiments show that, the developed CDR has an instantaneous bandwidth of at least 2.25 GHz. Its sensitivity value changes with the input signal frequency where it is observed to be -62 dBm at best and -41 dBm at worst through out the 2.25 GHz bandwidth. The one-signal dynamic range is reported as at least 60 dB for the whole band. The two-signal dynamic range changes according to frequency and its best and worst values are reported as 45 dB and 20 dB along the
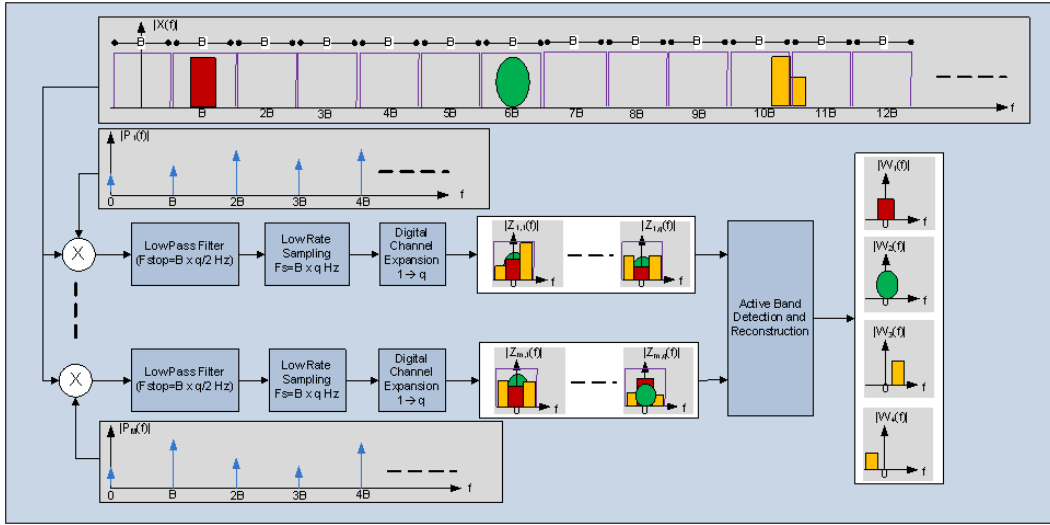
Fig. 1. Block schema of the Modulated Wideband Converter.

2.25GHz bandwidth, respectively.

The paper is planned as follows. In Section-II, the mathematical background on Modulated Wideband Converter is given. The implementation details of CDR are provided in Section-III. The experiment results and resource allocation table of the FPGA implementation of the OMP are given in Section-IV. Finally, Section-V is reserved for conclusions.

II. MATHEMATICAL BACKGROUND

Let $\mathcal{F}=[-F_{Nyq}/2, F_{Nyq}/2]$ be the operating frequency range of the MWC system whose block diagram is given in Fig.1. Assume that this range has been divided into $2L+1$ sub-bands of bandwidth B. Each sub-band has the following frequency support $\mathcal{F}_l=[lB-B/2, lB+B/2]$, $l=-L,..,L$, where the first and the last sub-bands satisfy the following conditions $-LB-B/2\geq -F_{Nyq}/2$ and $LB+B/2\leq F_{Nyq}/2$, respectively. Consider the following multi-band measurement model, which has P active bands:

$$x(t) = \sum_{p=1}^{P} a_p(t)e^{j2\pi Bl_p t}. \quad (1)$$

Here $l_p \in [-L, L]$ and $a_p(t)$ is the complex bandlimited signal satisfying $A_p(f)=0, \forall |f|\geq B/2$, where $A_p(f)$ is the Fourier transform of $a_p(t)$ defined as $A_p(f) = \int_{-\infty}^{\infty} a_p(t)e^{-j2\pi ft}dt$. Once $x(t)$ is received by the MWC, it is divided and fed into M identical analog channels, where in each channel $x(t)$ is multiplied by the real and periodic waveforms $p_m(t), m=1,..,M$. These waveforms are different from each other but they have the same period $T_p = 1/B$. Hence, each waveform have the following Fourier series expansion:

$$p_m(t) = \sum_{k=-\infty}^{\infty} c_{m,k}e^{j2\pi kBt}, \quad (2)$$

where $c_{m,k}$ is the kth Fourier series coefficient of the mth waveform, which can be computed as $c_{m,k}=B\int_{t_0}^{t0+1/B} p_m(t)e^{-j2\pi kBt}dt$ for any time instant t_0. Note that $c_{m,k}=c_{m,k}^*$, since $p_m(t)$ is real. The representative

spectra of $p_m(t)$ are shown as $P_m(f)$ in Fig.1. In each analog channel, before the analog low-pass filter the following signal appears:

$$y_m(t) = x(t)p_m(t) = \sum_{k=-\infty}^{\infty} \sum_{p=1}^{P} c_{m,-l_p+k}a_p(t)e^{j2\pi kBt}. \quad (3)$$

If the stop band frequency of the identical analog low-pass filters in each channel is chosen as $q\times B/2$, where q being the channel expansion factor [4], the resulting signals $v_m(t)$ at the end of each filter can be written as:

$$v_m(t) = \sum_{k=-\hat{q}}^{\hat{q}} \sum_{p=1}^{P} c_{m,-l_p+k}a_p(t)e^{j2\pi kBt}, \quad (4)$$

where $\hat{q}=(q-1)/2$. Note that analog filters are assumed to be ideal to simplify the formulation.

$$V_m(f) = \sum_{k=-\hat{q}}^{\hat{q}} \sum_{p=1}^{P} c_{m,-l_p+k}A_p(f + kB), \quad (5)$$

where $V_m(f)$ is the Fourier transforms of $v_m(t)$ respectively. Note that different linear combinations of $a_p(t), p=1,..,P$ signals appear at centre frequencies kB, $k=-\hat{q},..,\hat{q}$ in $v_m(t)$. To expand the number of channels by a factor of q, each channel is sampled at a rate $F_s \geq qB$ and multiplied by $e^{j2\pi q'Bn/F_s}, q'=-\hat{q},..,\hat{q}$ and a digital low-pass filter with cut-off frequency $B/2$ is applied. Hence, from each analog channel, the following q digital sub-band channel signals are generated:

$$v_{m,q'}[n] = (v_m(nT_s)e^{j2\pi q'BnT_s}), \quad q'=-\hat{q},..,\hat{q}, \quad (6)$$

where $T_s = 1/F_s$ is the sampling period of the ADC. Similar to analog filtres, digital low-pass filters are assumed to have ideal responses to simplify the formulation. (6) can be equivalently written in the spectral domain as:

$$V_{m,q'}(f) = \sum_{p=1}^{P} c_{m,-l_n+q'}A_p(f), \quad |f| \leq F_s/2. \quad (7)$$

Here $V_{m,q'}(f)$ is the Fourier transform of the digital signal coming from the q'^{th} digital sub-band channel of the mth
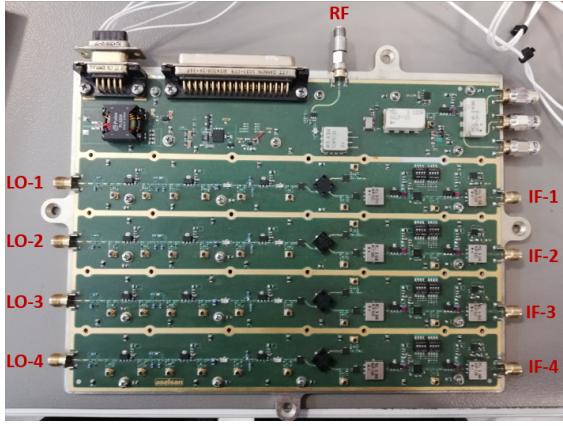
Fig. 2. RF-IF conversion card of the CDR.

Fig. 3. CDR setup.

analog channel. All the $M \times q$ channels have identical frequency response hence (7) can be written as the following linear system of equations:

$$\mathbf{v}(f) = \mathbf{C}\mathbf{b}(f) \qquad (8)$$

where

$$\mathbf{C}_{Mq \times 2L+1} = \begin{bmatrix} c_{1,-L-\hat{q}} & c_{1,-L+1-\hat{q}} & .. & c_{1,L-\hat{q}} \\ c_{1,-L-\hat{q}+1} & c_{1,-L+1-\hat{q}+1} & .. & c_{1,L-\hat{q}+1} \\ . & . & .. & . \\ c_{1,-L+\hat{q}} & c_{1,-L+1+\hat{q}} & .. & c_{1,L+\hat{q}} \\ c_{2,-L-\hat{q}} & c_{2,-L+1-\hat{q}} & .. & c_{2,L-\hat{q}} \\ . & . & .. & . \\ . & . & .. & . \\ c_{M,-L+\hat{q}} & c_{M,-L+1+\hat{q}} & .. & c_{M,L+\hat{q}} \end{bmatrix},$$

$$\mathbf{v}_{Mq \times 1}(f) = \begin{bmatrix} V_{1,-\hat{q}}(f) \\ V_{1,-\hat{q}+1}(f) \\ . \\ V_{1,\hat{q}}(f) \\ V_{2,-\hat{q}}(f) \\ . \\ . \\ V_{M,\hat{q}}(f) \end{bmatrix}, \mathbf{b}_{2L+1 \times 1}(f) = \begin{bmatrix} b_1(f) \\ b_2(f) \\ . \\ . \\ b_{2L+1}(f) \end{bmatrix},$$

(9)

$\mathbf{b}(f)$ is P-sparse, with the following non-zero entries $\mathbf{b}_{l_p+L+1}(f) = A_p(f), p=1,..,P$. For the discrete set of frequency values $f_n, n = 0, 1, .., N-1$, where $f_n = F_s n/N$, a multiple measurement formulation of (8) can be constructed as:

$$\mathbf{V} = \mathbf{C}\mathbf{B}, \qquad (10)$$

where $\mathbf{V} = [\mathbf{v}(f_0), .., \mathbf{v}(f_{N-1})]$ and $\mathbf{B} = [\mathbf{b}(f_0), .., \mathbf{b}(f_{N-1})]$. Given the multiple measurement vector $\mathbf{V}$ and the system matrix $\mathbf{C}$, the sparsest (block sparsity) $\mathbf{B}$ satisfying (10) is to be found. There are many fast greedy algorithms for solving (10) [7], [8]. Note that, by multiplying both sides of (10) with the inverse DFT matrix from the right, would enable to work with time domain samples rather than the spectral slices.

III. HARDWARE IMPLEMENTATION

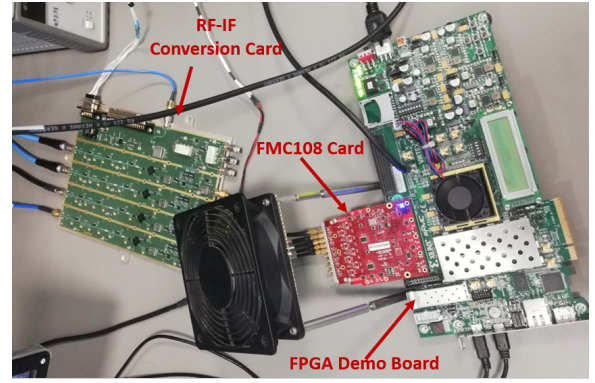Developed CDR has two main components: i)Analog Processing Block and ii)Digital Processing Block. The first component is the RF (Radio Frequency)-IF (Intermediate Frequency) conversion hardware. The second component is a FPGA (Field Programmable Gate Array) demo board, on which the compressed data is digitized and real-time reconstruction is applied to the generated samples. Randomization waveforms are generated using a Arbitrary Waveform Generator, where the subband bandwidth is set to 25MHz.

A. Analog Processing Block

Analog processing block is actually an RF-IF conversion card. A picture of this card is given in Fig 2. This card has one RF signal input port, four LO (Local Oscillator) signal input ports and four IF signal output ports. There are also control interfaces. The input RF signal is divided in to four identical channels. Each channel is composed of filters, attenuators, amplifiers, test points, etc. Once the RF signals on every channel are passed through this RF strip, they are mixed with the corresponding randomization waveforms ($p_m(t)$) coming from the LO ports of the card. On the LO path of each channel, there are multiple equalizers for balancing powers of the harmonics of the LO signals, appearing at every 25 MHz. On the mixer outputs, there are low- pass filters with stop band frequency of 125 MHz and digitally controllable attenuators and amplifiers to tune the amplitude level of the IF signal to be sampled by the ADC (Analogue-to-Digital) without being saturated. At the end of each analog channel, a spectrally compressed IF signal of bandwidth 125 MHz is generated. These signals are to be digitized and further processed by the Digital Processing Block, which will be detailed next.

B. Digital Processing Block

Digital Processing Block is composed of a balcony card which includes 4 ADCs operating at 250MHz sampling rate and 16 bit resolution, and KCU105 FPGA Demo Board. The balcony card is plugged to the demo board. Four IF outputs of the Analog Processing Block are connected to the inputs of balcony card. Generated samples are transferred to the FPGA for processing. CDR setup is shown in Fig. 3. To increase the number of digital channels, as discussed in Section-II, frequency translation and low pass filtering are applied digitally. Hence, the number of the digital channels are increased to 24, each of which has a data rate of 30.25 MHz
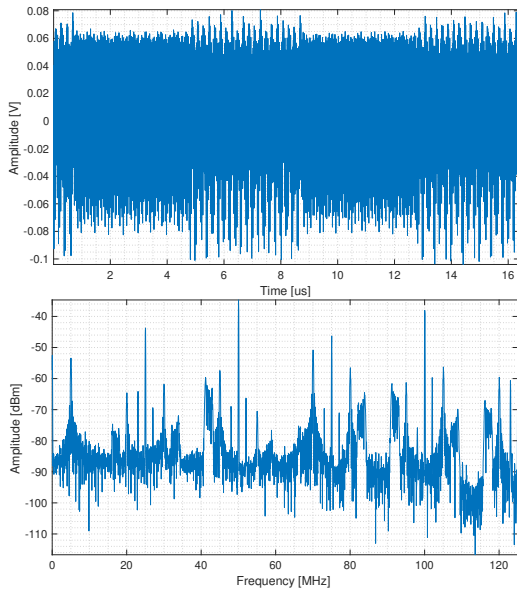
Fig. 4. Compressed data from the first ADC (top) and its spectrum (bottom).

Fig. 5. Recovered baseband signals (top) and their corresponding spectrum (bottom).

and caries a complex data. Then, OMP algorithm implemented on FPGA is deployed that solves the linear system of equations given in (10) for reconstruction.

IV. EXPERIMENTAL RESULTS

For measuring the instantaneous bandwidth, one/two signal dynamic range and sensitivity values of the CDR, first online system calibration procedure detailed in [9] is deployed and the system matrix $\mathbf{C}$ given in (10) has been filled.

For the instantaneous bandwidth measurement, RF output of three signal generators have been combined with a power combiner. Output of the power combiner has been connected to the RF input of the CDR. The signal generators have been adjusted such that the following waveforms are generated: i) CW (Continuous Wave) signal with center frequency 258 MHz, amplitude -35 dBm, FM (Frequency Modulation) bandwidth 2 MHz and FM rate 2 kHz; ii)CW signal with center frequency 2502 MHz, amplitude -25 dBm; iii) Pulse signal with center frequency 1505MHz, amplitude -30 dBm, pulse width 4 us and pulse repetition interval 8 us. Note that since two of the generated signals are CW, when the pulse signal is active, thee signals overlap in time, which is a very rare situation in a typical EW scenario. By choosing the center frequencies of the signals as 258 MHz, 1505 MHz and 2502 MHz, we aimed to validate that the CDR has an instantaneous bandwidth of at least 2250 MHz. All the data acquisition and recovery processes have been utilized in FPGA and they work in real time. To demonstrate the results, the acquired compressed data and the recovered baseband signals for 16us interval have been transferred to the computer from the Ethernet connection of the FPGA demoboard. The acquired compressed data from the first ADC and the corresponding spectrum are shown in Fig. 4. As observed the measured compressed signal is highly aliased, very complicated and it is very hard to recognize the waveforms coming from the signal generators. The recovery
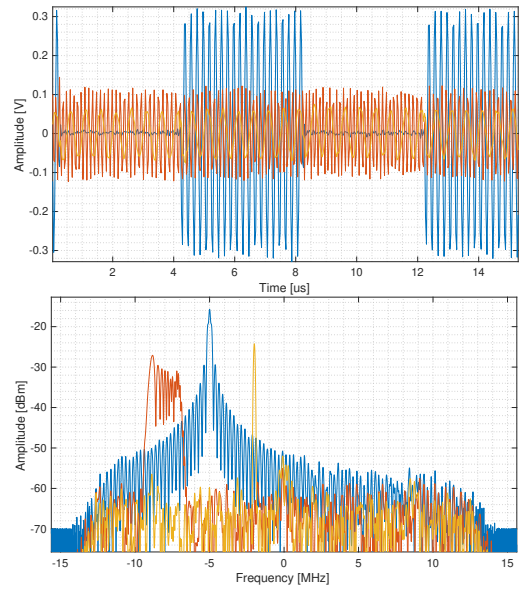
algorithm has detected 3 sub-bands with center frequencies 250 MHz, 1500 MHz and 2500 MHz for each sample. The recovered baseband signals, which are grouped based on their detected center frequencies, and their corresponding spectrum are plotted in Fig. 5. As observed baseband signals of all three waveforms together with their centre frequencies have been recovered successfully.

For measuring the sensitivity level of the CDR, a single signal generator has been connected to the RF input of the CDR. The signal generator parameters have been adjusted such that a CW signal is generated. The center frequency of the signal has been swept from 253 MHz to 2503 MHz with 25 MHz step sizes. For each frequency values, the amplitude level of the signal has been swept from -80 dBm to 0 dBm with 1 dB step sizes. For each frequency and amplitude pair, the real time recovery results of the approximately 10 us data (300 revored data sample) have been transferred to the computer. The probability of correct recovery for each amplitude-frequency pair is computed by dividing the number of correct centre frequency recoveries by 300. The resulting probability of correct recovery performance of the CDR as function of input signal frequency and amplitude level is shown in Fig. 6 on the top. The sensitivity curve of the CDR can be constructed by finding the minimum amplitude level for which the probability of correct recovery is higher than 0.99 for each frequency value. As observed, the sensitivity value of the CDR changes with respect to the frequency and has best and worst values of -62 dBm and -41 dBm through out the 2250 MHz bandwidth, respectively.

For two signal dynamic range measurement, RF output of two signal generators are combined using a power combiner and injected into to the CDR. From the first signal generator, a CW signal with fixed center frequency 2508 MHz and amplitude level 0 dBM has been given. The frequency and the amplitude level of the CW signal given from the second signal
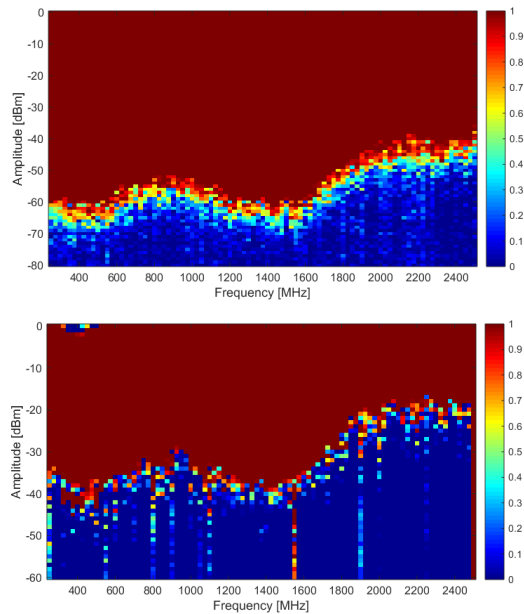
Fig. 6. Probability of correct recovery graphs for the sensitivity (top) and two-signal dynamic range measurements(bottom).

generator has been swept from 256MHz to 250 6MHz with 25 MHz step size and from -60 dBm to 0 dBm with 1 dB step size, respectively. Similar to sensitivity test, for each frequency-amplitude pair of the second signal, an approximately 10 us data has been acquired, the probability of correct recovery is computed based on the recovery results. Note that correct recovery in this test is defined as the successful recovery of the subband indices of both signals. Obtained probability of correct recovery graph as a function of frequency and amplitude level of the second signal is shown in Fig. 6, on the bottom. As observed, two-signal instantaneous dynamic range value of the CDR has best and worst values of 42 dB and 20 dB through out the 2250MHz bandwidth, respectively.

All the polyphase filtering and recovery processes are running in real time on the FPGA. The clock frequency of the FPGA is 250MHz. Polyphase filtering operation which generates 24 digital sub-band channels at a rate of 30.25 MHz each, is straight forward. On the other side, the implementation of OMP algorithm in FPGA is very complicated since the algorithm is iterative and requires computation of matrix inverses in each iteration. By optimizing the OMP algorithm for memory/computational resource usage and utilizing some simplifications on the algorithm (applying matrix inversion lemma, binomial series expansion for avoiding fixed point divisions, etc.), the algorithm has been successfully implemented on FPGA. For each acquired sample, the algorithm runs for 3 iterations (for recovering maximum 3 signals), where in the last iteration inverse of a 6x6 matrix is computed. The details of the OMP implementation on FPGA are given in [10]. The FPGA resource utilization in terms of number of LUTs (Look Up Table), FFs (Flip Flops), DSPs (Digital Signal Processing Element) and BRAMs (Block Ram) used are given in Table

TABLE I
RESOURCE ANALYSIS OF FPGA IMPLEMENTATION OF OMP ALGORITHM

	LUT (K)	FF (K)	DSP	BRAM (36K1)	Max. Clock Freq.(MHz)	Latency (ns)	MSE (dBFS)
$M=24, N=10$	22.8	22.0	392	85.5	216.7	941.5	-75.6
$M=24, N=50$	59.9	41.2	914	185.5	216.7	941.5	-75.6
$M=24, N=100$	106.9	65.1	1562	310.5	216.7	941.5	-75.6
$M=24, N=10$	24.0	24.1	392	85.5	216.7	941.5	-81.7
$M=24, N=50$	62.3	43.7	914	185.5	216.7	941.5	-81.7
$M=24, N=100$	110.3	68.3	1562	310.5	216.7	941.5	-81.7

1. In the table, M and N represent the size of the complex dictionary $\mathbf{C}$. The first three and the last three rows show the obtained results for carrying 16 bit and 18 bit fixed point arithmetic operations in FPGA, respectively. The Max Clock Frequency and Latency columns represent the maximum clock frequency achived and the resulting latency for the given M, N values, respectively. The last column MSE (Mean Square Error), displays the error between recovery results obtained from fixed point FPGA recovery and the double precision computer recovery. Using 18bit fixed point arithmetic provides better MSEs, as expected.

V. CONCLUSIONS

In this work, sensitivity, one/two-signal dynamic range and instantaneous bandwidth measurement results of the recently developed Compressive Digital Receiver (CDR) hardware for Electronic Support Measures (ESM) applications, is reported for the first time. The developed CDR has its own RF-IF conversion card. The digital processing part has been carried on a FPGA demo board. All the digital processing including real time recovery has been implemented in FPGA. The obtained results show that the developed hardware can be effectively used in an ESM system as a digital receiver.

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