DESIGN OF A LOW−POWER DAC SYSTEM FOR WLAN 802.11 WIRELESS TRANSMITTERS

Author(s):
Nicola Ghittori (University of Pavia, Italy)
Andrea Vigna (University of Pavia, Italy)
Vincenzo Ferragina (University of Pavia, Italy)
Piero Malcovati (University of Pavia, Italy)
Stefano D'Amico (University of Lecce, Italy)
Andrea Baschirotto (University of Lecce, Italy)

Abstract:
Present and up−coming WLAN applications need the cascade of a digital interpolator filter, a DAC and a smoothing filter in the transmitter baseband section. This paper presents the design of a baseband architecture with a high conversion rate that enables the use of a passive filter at the output of the DAC to suppress its spectral images. The use of an active reconstruction filter is so avoided, with a benefit in terms of linearity and power consumption. The proposed architecture has been implemented in a 0.13−um CMOS technology with a 1.2−V supply voltage and simulated at a fully−transistor level. In particular the DAC, operating at 600 MHz, has a power consumption as low as 2.4 mW and achieves a FS SFDR higher than 66 dB for input signal frequencies up to 10 MHz and a FS dynamic range of 10 bits in the WLANa/g 10−MHz bandwidth.