From AVC Decoder to SVC: Minor Impact on a Dataflow Graph Description (Abstract)
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Pipelining Architecture Design of the H.264/AVC HP@L4.2 Codec For HD Applications (Abstract)
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New LZW Data Compression Algorithm and Its FPGA Implementation (Abstract)
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Algorithm and Architecture Design for Intra Prediction in H.264/AVC High Profile (Abstract)
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FLEXIBLE ARCHITECTURE OF PROCESSOR OPTIMIZED FOR MULTIMEDIA APPLICATIONS (Abstract)
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Area-efficient Quantization Architecture with Zero-prediction Method for AVS Encoders (Abstract)
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VLSI Architecture of H.264 RDO-based Block Size Decision for 1080 HD (Abstract)
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**Topic:** Implementation architectures and VLSI

**A Hardware-oriented Intra Prediction Scheme for High Definition AVS Encoder** *(Abstract)*
Man-Lan Wong, Yi-Lun Lin, Homer H. Chen

**A 158 MS/S JPEG 2000 CODEC WITH A BIT-PLANE AND PASS PARALLEL EMBEDDED BLOCK CODER** *(Abstract)*
Masayuki Miyama, Yuusuke Inoie, Takafumi Kasuga, Ryouichi Inada, Masashi Nakao, Yoshio Matsuda

**LOW-POWER HIGH-THROUGHPUT MQ-CODER ARCHITECTURE WITH AN IMPROVED CODING ALGORITHM** *(Abstract)*
Alireza Aminlou, Maryam Homayouni, Mahmoud Reza Hashemi, Omid Fatemi