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Flexible Development and Testing Environment for Implementation of new Algorithms in RFID Systems

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***Abstract*—This paper presents a rapid-prototyping platform for test and implementation of new algorithms in RFID Systems. The platform offers the possibility to evaluate and test new approaches, in communications aspects in RFID systems, that can not be tested in state-of-the-art systems, due to hardware or standards limitations. This includes new radio architectures, source-/line-coding schemes, multiple access control algorithms and many other system elements that can not be accessed or changed in a RFID system. Two platforms are presented: one for algorithm development and a second one for product development.**

***Keywords*-UHF RFID; Rapid Prototyping; SDR;**

I. Introduction

A. Radio Frequency Identification

Radio frequency identification (RFID) systems use radio waves in order to retrieve the identity of an object wirelessly. They are grouped under the broad category of automatic identification technologies. Unlike bar-code technology, RFID technology does not require physical- or optical contact for communication. RFID data can be read through the human body, clothing and non-metallic materials.

The main parts of an RFID system are: the reader which manage the communication and the tags which are the identifiable devices attached objects. RFID systems are basically divided into active and passive. In passive systems the tags use the energy of the electromagnetic field radiated by the reader as energy source and as carrier for the data transmission. Active tags are provided with energy by local means. The RFID systems work in LF, HF, UHF frequency bands [16].

In the last years RFID has evolved into an active multi-disciplinary area of research and development, composed by a broad spectrum of fields. The tasks of RFID tags have become more complex, this includes:

- Tags are placed in reflective environments.
- Tags are provided with sensor capabilities used to monitor specific processes.
- Higher data rates are needed in systems where the tag sends more than just its ID, i.e. sensor tags.
- The reliability of RFID systems has to be increased. The user needs to be sure that all tags are read at all times.

All these challenges have open the doors for research and development in the areas of RFID. Now a days RFID system are being investigated all over the world. Many algorithms and technologies of other communication areas are being applied to RFID systems. Nevertheless in order to evaluate new ideas in RFID a prototyping system is needed, one which provides flexibility and the possibility to work outside of the standards and state-of-the-art systems.

B. Software Defined Radio

The concept of Software Defined Radio, for now on referred as SDR, describes a system where the processing of the RF signal takes place in the digital domain. Ideally an ADC (Analog Digital Converter) is connected directly to the antenna. The digital signal processing and protocol implementation are defined in software, enabling the possibility for configuration and optimization without the need of changing any hardware components. The SDR approach is already present in many of the actual communications systems, and is becoming strong as a solution for future telecommunication implementations [5].

An SDR solution brings some advantages to a system, it makes it reconfigurable and reprogramable, even in operation; An SDR-based system can be updated to new standards by just changing the software. However, a fully SDR system requires a high performance level on the Analog digital converter and the signal processor.

C. SDR in RFID

The idea of using SDR in RFID for prototyping has been already explored in different publications. As examples [8], [9], [10], [11], [12] and [13]. In this publications the authors have used the flexibility of SDR to test new coding schemes, radio architectures, channel equalization, new modulation schemes, MIMO approaches and other research activity.

In [3] a flexible simulation and prototyping for RFID designs was presented, most of the signal processing take place in software, nevertheless the system has some restrictions:

- The FPGA (Field Programmable Gate Array) has very limited resources compared to more modern FPGAs.
- The FPGA board board is part of factory-defined system. Many of the components are fixed and can not be changed. This may present some restrictions.
- The analog front-end is fixed. One front end for HF and UHF systems.

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II. Rapid Prototyping Platform

This paper presents a rapid-prototyping platform for test and implementation of new algorithms in RFID Systems. This section gives a basic description of the main elements and capabilities of the platform. Two platforms have been developed. One for research and development and another one for fast product-prototyping.

A. Requirements

The platform should have the following characteristics:

- *Modular construction*: the main components of the platform should be interchangeable. This applies for hardware and software elements.
- *Flexible*: the platform should provided with a variety of possibilities for the signal processing.
- *Re-programmable*: the platform should be reusable by simple means.
- *High performance*: as part of the flexibility, the resources of the platform should not present a close limitation on the algorithm development.
- *Short time-to-prototype*: the complexity of stepping the test platform to a possible prototype should be kept as minimum as possible.

B. Structure

The Figure 1 presents an overview of the main components of the test platform. The main element is the FPGA which is where the signal processing takes place. There is a fast digital interface where sender and receiver can be connected to. The PC can communicated with the FPGA in order to configure it of control a certain action. The sender and receiver configuration depends on the RFID technology in use.

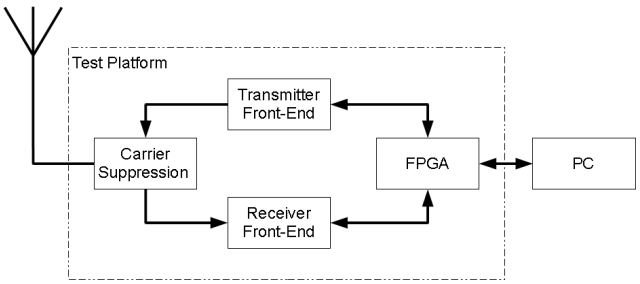

Figure 1. Overview of the Test Platform

C. Hardware Elements

1) Signal Processor: In the center of the test platform is the signal processor. The signal processing is done in the digital domain, this adds flexibility to the system. The processing algorithms are defined in software. I.e. the signal processor can realize different tasks by just changing the running program. This reduces the time cost for test and implementation.

FGPA: The signal processor chosen for the test platform is an FPGA . The FPGAs are programmable logic elements than can be configure to work as any digital circuit. Different elements can be programed to work in parallel, this makes them a feasible way to defined radio elements (demodulators, filters etc) in software. The FPGAs used in both boards have a high number of logic elements. The Spartan 3 DPS used in the development board has 126 hardware multipliers and 23,872 slices while the XC2V2000 used in [3] has 56 multipliers and 10,752 slices. The Virtex 6 FPGA used in the development has 768 hardware multipliers and 37,680 slices [26].

2) Analog Digital Converter: To add flexibility to the system, most of the signal processing would take place in the digital domain. Therefore an analog to digital converter (ADC) works as interface between the analog signal processing and the digital signal processing. There are two ADC modules that can be adapted to the test platform, their use depends on the desired configuration of the system.

12 bits @ 500 MSPS: One of the ADC modules can sample signals up to 500 MSPS (Mega Samples Per Second) and has a resolution of 12 bits. The resolution of this ADC module could be of a disadvantage when sampling signal with a high dynamic range. But at the same time it allows to sample signals with high frequency components. It also has a relative high bandwidth which makes it suitable for sampling RF signals directly by means of undersampling techniques. Figure 2 shows a photograph of the ADC module.

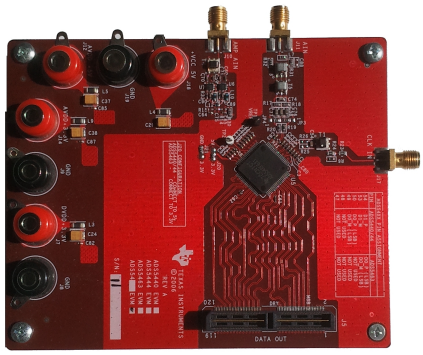

Figure 2. 12-bits ADC [27]

16 bits @ 105 MSPS: The second ADC module has a bigger dynamic range (higher resolution). It is a quite suitable for sampling signals with small power levels and lower frequency components. Figure 3 shows a photograph of the ADC module.

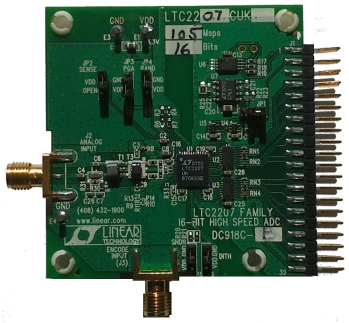

Figure 3. 16-bits ADC [28]

Analog Front-End: The analog front-end depends on the system, there are front-ends for LF, HF, and UHF that can be connected to the processor board.

D. Software Elements

1) ADC Interface: The communication between FPGA and the ADC is realized in this module. It can be easily configure for different data rates and bit widths.

2) Base Band Generator: The base band generation takes place in the FPGA. Here the digital signal is channel coded and passed through a symbol former. The base band generator delivers two signals: In-phase and Quadrature (I and Q). In this way different modulation schemes are supported. This software module can be used to generate any base band needed.

3) Receiver Digital Front-End: The digital front-end module uses an CIC (Cascade Integrator Comb) for filtering and decimating. Figure 4 shows the block diagram of the digital front-end.

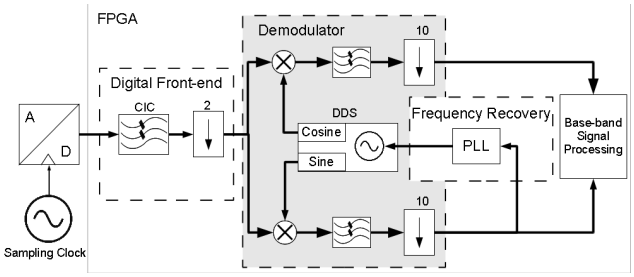

Figure 4. Digital Front-End Flow Diagram

Decimation: In a digital communication system the bandwidth of the received signal is typically smaller than the resulting bandwidth after the sampling process. This bandwidth is called the *Nyquist Bandwidth* and it corresponds to $\frac{f_s}{2}$. Therefore the first step on a digital receiver is a decimation block, this one re-sample the received signal with a slower sample frequency. In other words it discards a certain number of samples out of the received signal. The CIC (Cascade Integrator Comb) is a digital filter structure with a low-pass filter frequency response. The reader is directed to [17] and [24] for more information on CIC filters.

Implementation: CIC filter can be used directly out of the Xilinx libraries. All parameters can be configured within a graphical environment. Nevertheless a VHDL module for CIC filters is provided by the author.

Demodulator: The received signal can be ASK or PSK modulated. Therefore an In-phase/Quadrature (I-Q) demodulator was programed. The IQ demodulator provides a coherent measurement of the phase and magnitud of sinusoidal signals [17]. The IQ demodulator is the most used demodulation architecture, nevertheless other demodulation architectures can be made based on this module.

Implementation: It requires two multipliers, an oscillator and phase shift element for the 90 degrees shifted signal. The FPGA has dedicated hardware multipliers that can be used directly. For the oscillator an element called DDS (Direct Digital Synthesizer) is used. The DDS is taken from the Xilinx libraries, it generates sinusoid signals with a configurable frequency. The DDS provides directly with a cosine and sine signal that can be used to generate the I and Q paths.

Low-pass Filter: The low-pass filter eliminates the harmonics generated by the multiplication of two sinusoids. It is implemented using the FIR (Finite Impulse Response) generator from the Xilinx libraries. The filter is also used for decimation; the signal bandwidth is limited by the cut frequency of the filter after the demodulator. Hence the signal can be re-sample to a quite lower frequency, relaxing the processing requirements of the further processing blocks.

4) Frequency Recovery: The I-Q demodulator is a coherent demodulator. Therefore it requires to know the frequency of the carrier signal in advance, the phase is irrelevant hence it is contained in the I and Q signals. A frequency recover element is often necessary. Here a PLL (Phase Locked Loop) is used. A PLL is basically a control loop that regulates the frequency of the oscillator until the carrier frequency is matched. Figure 5 shows the block diagram of the implemented PLL.

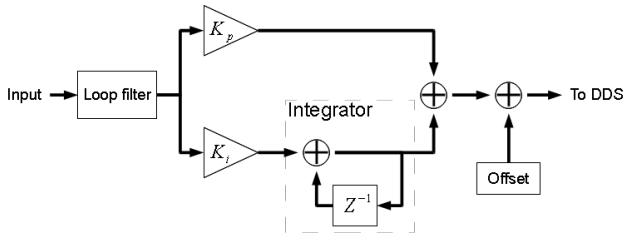

Figure 5. PLL Block Diagram

Implementation: The quadrature path is used as phase discriminator, the PLL regulates the DDS until quadrature path converges to 0. In other words, when the phase of the carrier and the one from the DDS are the same, the DC offset of the quadrature signal is zero. This structure keeps the DDS at the same frequency as the incoming carrier. The PLL is programed in VHDL, the modules are configurable and can be used in different arranges. See Figure 5.

E. Characteristics

The test platform offers a flexible environment to test and implement new algorithms for RFID systems. The digital processing elements are logic modules described in software. Most of the system elements are defined with programmable logic.

Advantages:

- The digital processing elements are configurable and reusable.
- The digital processing elements can be used stand-alone or be included in a bigger system.
- New modules can be easily described and added to the system under test.
- Different receiver architectures can be tested parallel.

III. Programming and Communication

This section describes how the Rapid Prototyping platform is used.

A. Module Description

The signal processing modules can be described using either VHDL or Verilog. The ISE software form Xilinx offers a complete environment for logic description. Basically any HDL generator compatible with Xilinx devices can be used.

B. Configuration

The FPGA configuration is made via the USB-JTAG port. This interface is also used for the ChipScope communication.

C. PC Interface

The test platform includes an USB-Serial module that allows to connect the Board to the PC through an USB port. At the PC this port is seen as a virtual serial port. This interface can be used to communicate with FPGA by means of a serial terminal.

Datapoints and Parameters:: There is a Wishbone-like data bus implemented in the system. Basically there are two memory arrays: one for control and one for status. The registers in the control array are input signals or parameters into the system, whereas the status array are output signals of the system. These two memory array can be used to configure a module, trigger a task of to get information out of the system.

Protocol:: By using the USB-Serial port the PC can write data into the control array and in the same way read data out of the status array. The protocol is simple, the first byte in a message tells the Wishbone whether to write or read, the second bytes tell how many bytes and a third byte gives the address of the memory array.

D. Visualization

ChipScope:: ChipScope tool inserts logic analyzer, system analyzer, and virtual I/O low-profile software cores directly into the design, allowing to view any internal signal or node, including embedded hard or soft processors. Signals are captured in the system at the speed of operation and brought out through the programming interface. Captured signals are then displayed and analyzed using the ChipScope Pro Analyzer tool. [26]

Test-points:: The USB-Serial port of the test board can be used to transfer data to the PC. A VHDL module allows the storage and latter transfer the data of a test point in the system. In this way test-points can be added internally in the system and visualized in the PC.

IV. Development Platform

In this platform many of the elements are not fixed and can be arrange as required. The board it is provided with a high performance FPGA. The Virtex 6 evaluation board offers a lot of digital interfaces that can be used as required. The resources of the FPGA are extensive and can be used to implement big systems. Figure 6 shows a photograph of the FPGA development board.

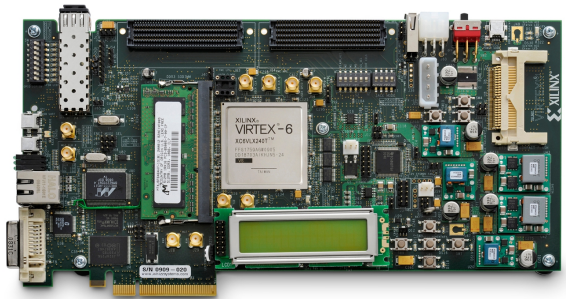

Figure 6. Virtex 6 Evaluation Board [26]

The ADC can be connected to this board by means of adapter boards. An UHF sender has been already developed that can be connected to the Virtex 6 board.

UHF Sender:: This module can be used in UHF RFID systems, it supports the frequency spectrum and power level specified by the standards. This sender is quite flexible, never the less all components are fixed, this sender module can be used as base for constructing other senders with specific capabilities. The digital interface to the FPGA board is quite flexible. Figure 7 shows a block diagram of the sender.

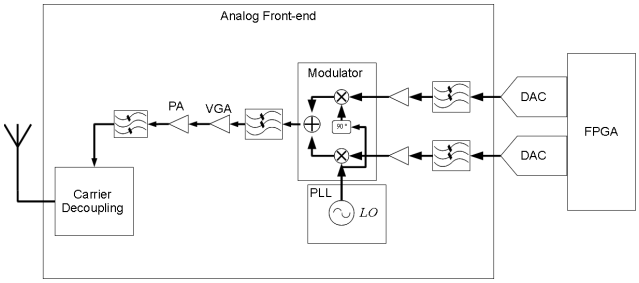

Figure 7. Block Diagram of the Sender

Figure 8 shows a photograph of the sender PCB (Printed Circuit Board). The sender board can be connected directly to the Virtex 6 evaluation board through a high-speed digital interface.

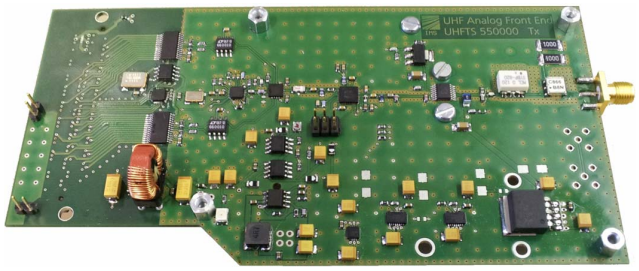

Figure 8. Complete Sender Board with FPGA Interface

Figure 9 shows a photograph of the test platform, it can be seen how the ADC and the sender are connected to the Virtex 6 board.

A. Example: UHF RFID Reader

Using this platform an UHF RFID reader was developed and presented in [7] and [14]. This system is capable of readying standard tags. The protocol state machine, the radio receiver and the base band processing take place on the FPGA as well. This system has been used to test a new channel coding scheme for tag-reader communication as well, it is published in [15]. An undersampling scheme for direct digitization was implemented and test in this platform see [7].

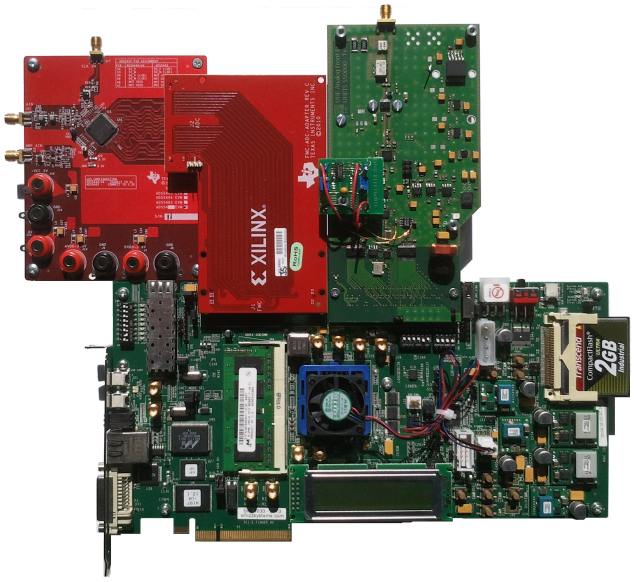

Figure 9. Picture of the Test Platform

V. Product Platform

Once a system is tested and evaluated it can be implement in a smaller and low-cost platform. A digital signal processing module has been developed for special use in RFID. The module has a fast digital signal interface, a DSP specialized FPGA and a Cortex M3 micro controller. Figure 10 shows a photograph of the digital processing module.

The idea is to used the digital interface to connect an application specific analog module. According to the RFID application, the analog module takes care of the signal processing task that can not be done in the digital module. The ADCs and DACs are contained in the Analog module as well.

A. Example: HF RFID System for Heart Sensors

Application specific HF RFID reader was developed, which can read pressured sensors implanted in the heart. The system is not standard compliant and requires special signal processing for the recovery of the data. The system was first developed in the development platform and then ported to the product prototyping platform. For this task an analog module was developed as well. Figure 11 shows a photograph of the system, on the right the DSP module and on the left the corresponding analog module. Please refer to [18], [19], [20], [21], [22] and [23] for more information on the system.

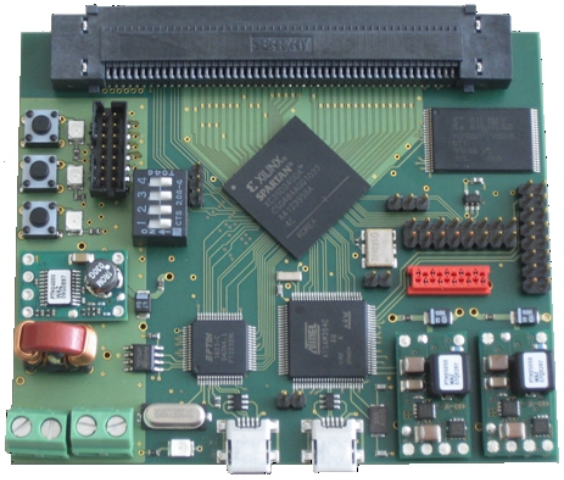

Figure 10. Picture of the Product-Prototyping Platform

Figure 11. Picture of the Heart Sensor UH-RFID Reader

VI. Conclusions and Outlook

A rapid-prototyping platform for RFID research and developed was presented. The development system has been used UHF and HF RFID systems. The system is flexible and modular, it can be used to evaluate and test new system algorithms. An product prototype for an HF RFID reader was already developed using the rapid-prototyping platform. The hardware and software modules are not limited to RFID, it could be used for other communications systems as well. [1]

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