Low–Power CMOS Voltage Regulator Architecture for Implantable RF Circuits

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***Abstract*—We present design architecture of a low–power voltage regulator that includes a charge–pump and a bandgap voltage reference in CMOS 130nm technology. The DC regulator is intended for RF IC energy harvesting applications and optimized for powering implantable electronics. The internal circuit sections work with the local power supply voltage levels in the 1.5V to 1.9V range (worst case), and the 3.96uW bandgap generates 462mVDC reference voltage. The complete regulator consumes typically 18uW for its own operation while delivering regulated V(PWR)=1V voltage within 0.14% variation under full load conditions, i.e. I(PWR)(max)=4mA current.**

***Keywords*-Analogue IC, implantable sensors, telemetry, energy harvesting**

I. Introduction

Realistic design constrains for implantable telemetry systems are driven by the subject's body size and the implant's power consumption. Larger subjects (e.g. a cow or a human) can accept an implant whose volume is in the order of a few tens of cubic centimetres, while a tiny mouse body can only accommodate fully implanted object with the volume in the order of a only few cubic millimetres.

For the case of small subjects, suitable power scavenging methodology is based on a short–distance inductive coupled wireless transfer of electromagnetic (EM) radiation [1] from the external energy source (larger inductor L_p) to the implanted receiving circuit by means of the smaller inductor L_{ins}, Fig. 1. However, the subject carrying the implant moves freely inside the controlled space, therefore the two inductors continuously change their relative position in space. Hence, the inductive coupling coefficient is function of both linear and angular displacements between the two coils, i.e. $M = f(d, \Theta)$, Fig. 2. Therefore, the received energy levels vary over a wide range. This situation poses a problem for normal operation of the implanted signal processing and communication electronics. Consequently, it is important to design an efficient implantable voltage regulator that also consumes a minimal amount of energy for its own operation while providing continuous power to the load.

In this paper we present our design architecture of a low–power voltage regulator, Fig. 1, that consists of the following sub–blocks: a) a rectifier/charge–pump; b) a closed–loop regulator consisting of an operational amplifier and

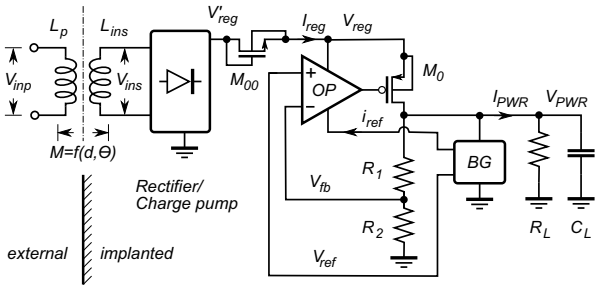

Figure 1. Block digram of energy harvesting front–end circuit showing the inductors, rectifier/charge pump and closed–loop regulation with amplifier and bandgap (BG) voltage/current reference, (the compensation $R_C C_C$ network not shown). We characterized the circuit operation both with M_{00} included, i.e. when $V'_{reg} \neq V_{reg}$, and without it, i.e. when $V'_{reg} = V_{reg}$.

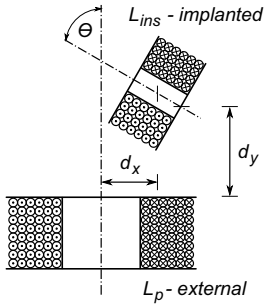

Figure 2. Diagram of two non–coaxial and non–parallel circular coils cross–section. Relative location, and therefore the coupling coefficient M, of the two power transfer coils (external and implanted) is defined by horizontal (d_x), vertical (d_y), and angular (θ) misalignments. (The plot is not to scale.)

$R_{1,2}$; and c) a temperature and power supply insensitive voltage/current reference. The rest of the paper is organized as follows: in Section II the inductive RF link and rectifier/charge pump are described. Section III contains a description of the regulator loop operation, voltage/current reference is described in Section IV, and concluding remarks are in Section V.

II. Voltage Rectifier

A recently adapted method of resonance–based power transfer [2] based on the coupled–mode theory [3] is less

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sensitive to changes in the distance between coils. Two pairs of coils are typically employed: one in the external circuit (in the driver, i.e. the primary coils), and the other in the implant itself (secondary coils).

Since the maximum power transfer can only be achieved when the external and implanted inductors are perfectly aligned, the challenge is to design a powering system that would have low sensitivity to the coil orientation and distance. Such designs, which are mainly focused on the generation of constant minimum power from the floor of the subject's cage, have been investigated in [4].

In our previous work, we investigated the effects of axial and angular misalignment of the primary and secondary inductors, which occurs due to the random movement of the subject, and presented numerical analysis methodology [5].

When L_1 and L_2 are the self–inductance of the two coils, M and k are related by

$$M = k\sqrt{L_1 L_2} \tag{1}$$

For two non–coaxial and non–parallel filamentary coils, the mutual inductance defined in is

$$M = \frac{\mu_0}{\pi}\sqrt{R_P R_S}\int_0^{\pi} \frac{(\cos\theta - \frac{d}{R_S}\cos\phi)\Psi(k)}{\sqrt{V^3}}d\phi \tag{2}$$

For our case of multilayer helical coils with axial and angular misalignment, we apply the filament method [6] to (2) and calculate the mutual inductance, which produces the following equation:

$$M = \frac{N_1 N_2 \sum_{g=-K}^{g=K}\sum_{h=-N}^{h=N}\sum_{l=-n}^{l=n}\sum_{p=-m}^{p=m} M(g,h,l,p)}{(2S+1)(2N+1)(2m+1)(2n+1)} \tag{3}$$

where

$$M(g,h,l,p) = \frac{\mu_0}{\pi}\sqrt{R_P(h)R_S(l)}\times \int_0^{\pi} \frac{[\cos\theta - \frac{y(p)}{R_S(l)}\cos\phi]\Psi(k)}{\sqrt{V^3}}d\phi \tag{4}$$

while denotation of all variables in (2) to (4) follows [7].

Based on numerical analysis, the resonant based power transfer methods are expected to achieve maximum power at power efficiency of approximately 85%, while the maximum power efficiency is designed for a specific distance in between the two coils, for example $d_y = 40mm$ as in Fig. 3.

Most modern IC rectifier/charge–pump topologies are derived from the conventional multistage Dickson circuit [8], with modern variants based on self–V_{th}–cancellation (SVC) methodology published [9], where each two–diodes–two–capacitors stage acts as a voltage doubler, therefore contributing the $2(\hat{V}_{in} - V_D)$ voltage overdrive to the output, where $\hat{V}_{in}$ is the peak input voltage while V_D is the diode turn–on voltage, and the diodes are implemented by MOS

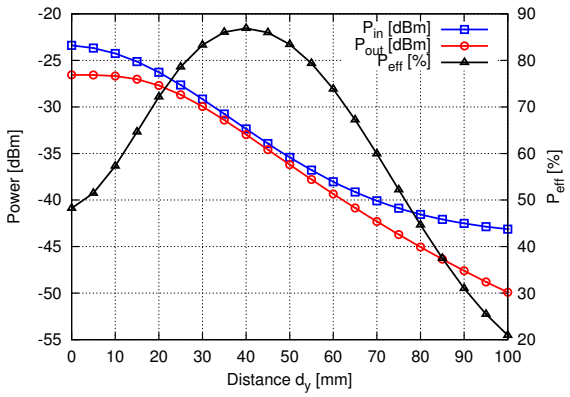

Figure 3. Simulated transmitted power vs coil distance d_y (case of perfectly aligned coils, i.e. $d_x = 0$ and $\Theta = 0$). Generated voltage is $V_{ins} \leq 1.5V$.

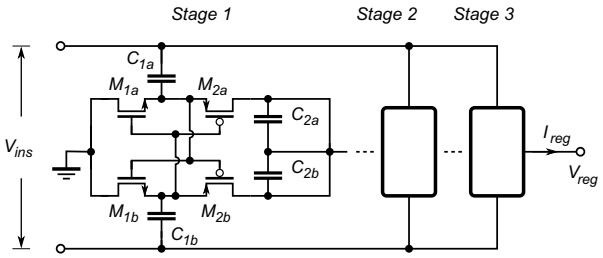

Figure 4. Schematic diagram of the three stage CMOS rectifier/charge pump.

devices in CMOS technology. Hence, V_D is equivalent to a MOS threshold voltage, $|V_{th}|$.

Our version of a three stage SVC type rectifier/charge–pump, Fig. 4, also uses the conventional NMOS as the base reference, and it was optimized for medical RF wireless band. It is interesting to note that if transistor M_{00}

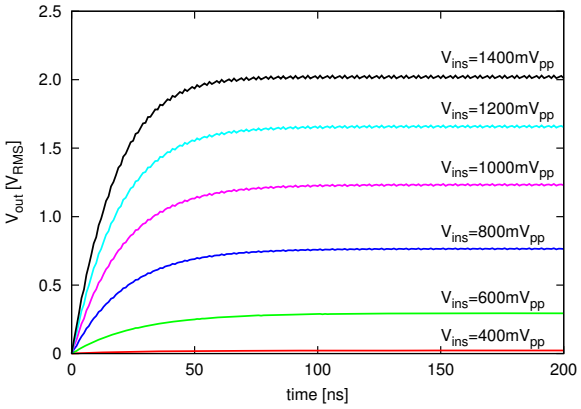

Figure 5. Simulated time–domain response of the rectifier/charge pump circuit without M_{00} transistor.

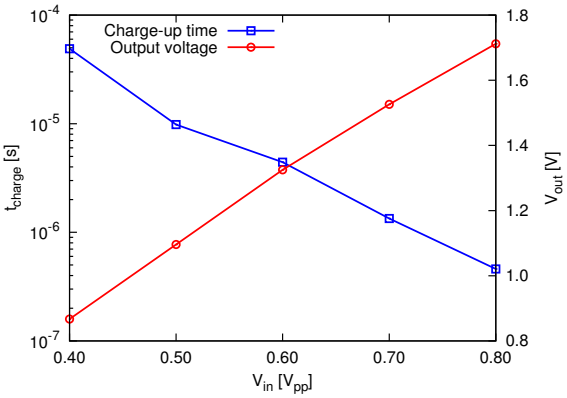

Figure 6. Time required for the regulated voltage to reach the steady DC level (note the logarithmic scale), and output vs. input voltage characteristics (note the linear scale). The graph demonstrates influence of the M_{00} transiator.

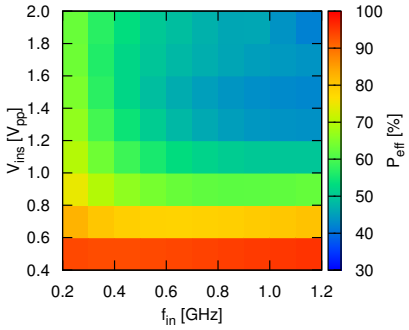

Figure 7. Simulated rectifier/charge pump efficiency vs. the input voltage V_{ins} and frequency.

is excluded (i.e. $V'_{reg} = V_{reg}$) then the rectifier output reaches constant level within less than 100ns for all input voltage levels, Fig. 5. However, if the M_{00} is included (i.e. $V'_{reg} \neq V_{reg}$ and there is voltage drop across M_{00} drain–source), the amount of time to charge up the internal nodes of this device and to reach steady output DC level varies exponentially from hundreds of nanoseconds (for high input voltage levels) to tens of microseconds (for low input voltage levels), Fig. 6. We will discuss compromises related to the use of M_{00} in more details latter in this text.

An important overall design compromise is the power efficiency of the rectifier circuit by itself, which is (for the given distance between the external and implanted coil) characterized as the function of the input RF signal frequency and the voltage V_{ins} generated across the implanted coil. Our design is, currently, optimized for frequency range between 400MHz and 1.2GHz, and the input voltage levels in between $600mV_{pp}$ to $800mV_{pp}$, Fig. 7. Under these conditions the power efficiency is more than 80%. Lower input voltage levels result in apparent higher efficiency (i.e. close to 100%), however the transistors are operating in sub–threshold region and, therefore, the total useful power drops by orders of magnitude, which creates the additional design constrain. For future implantable circuits that can operate in deeper sub $1mW$ power region this mode of operation may be more suitable.

III. Voltage Regulator Loop

The widely fluctuating voltage generated by the charge–pump is regulated by a series regulator, which by itself has to work with very low power and low–voltage [10], if it is to be useful for implantable medical telemetry systems. In the CMOS 130nm technology, the maximum potential difference that a device can tolerate is $1.5V$. Schematic block diagram of our regulator architecture, Fig. 1, shows that (in contrast to a conventional regulator) a source follower M_{00} is inserted between the charge–pump output node V'_{reg} and the rest of the regulator loop, while the PMOS M_0 is used as a pass device. Depending upon the power level of the input RF signal, the antenna gain, impedance matching, and the charge pump topology, the V'_{reg} voltage may rise above 1.5V. Hence, transistor M_{00} serves as a voltage limiter and lowers the V'_{reg} voltage level by V_{gs00}, which is load dependent and between $100mV$ to $400mV$. To make sure that the voltage between any two terminals of the NMOS M_{00}, e.g. its gate and bulk, stays within 1.5V even when V'_{reg} is higher than 1.5V, the M_{00} has its bulk and source shorted, which also improves the power supply rejection ratio (PSRR). If the incoming RF wave is held below 1.5V then M_{00} may not be used, so that the voltage drop across its drain–source is removed. However, in that case the overall PSRR of the regulator is reduced. That is, compromise between the voltage drop and PSRR is made based on the specific application conditions.

The regulation feedback loop is formed by the amplifier OP, the PMOS driver M_0 and the voltage divider R_1 and R_2 network, which sets the ratio between V_{PWR} and V_{ref} voltages as

$$V_{PWR} = \left(1 + \frac{R_1}{R_2}\right) V_{ref} \tag{5}$$

The voltage reference V_{ref} is then routed back to the input of the loop. The loop is designed to be stable with wide range of load impedances, with full load set up to $R_L = 250\Omega$ and $C_L = 50pF$. The maximum load corresponds to the maximum current drawn from V_{PWR}, which is designed to be $I_{PWR}(max) = 4mA$. By powering the reference circuit (BG) from V_{PWR}, the overall PSRR of the V_{ref} is further improved. In this design, the regulated supply voltage is set to $V_{PWR} = 0.985V$ while the complete regulator consumes less than $11.6\mu A$ current (typically). The

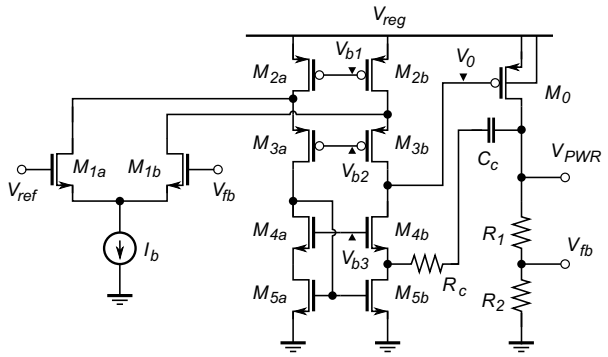

Figure 8. Schematic diagram of the folded amplifier (OP) used in Fig. 1 (with the compensation $R_C C_C$ network, transistor M_0, and $R_1 R_2$ explicitly shown again for clarity).

reference voltage also serves as a load to the regulator loop, which helps to keep the loop stable when its load is at the minimum.

Simplified schematic diagram of folded–cascode amplifier, Fig. 8, also shows the internal biasing voltages V_{b1}, V_{b2}, V_{b3} and biasing current I_b (details of the biasing circuit generator are not shown). In our CMOS 130nm process, the threshold voltages $V_{tn} \approx 0.15V$ to $0.25V$, and $|V_{tp}| \approx 0.23V$ to $0.4V$. Assuming approximately $0.275V$ headroom for the cascoded PMOS devices and $0.175V$ headroom for the cascoded NMOS devices, the cascoded branch requires at least $0.9V$ supply, while the other branches have smaller number of stacked devices. Hence, we designed the biasing circuit generator V_{b1}, V_{b2}, V_{b3} to set the minimum power supply level while ensuring that the associated devices operate in their respective saturation region under all variations of the input voltage levels.

By setting the biasing current for each of the top PMOS branches to $1\mu A$ and the input differential pair to its subthreshold region, the amplifier consumes the total current of $4.7\mu A$, including the bias circuit generator. The DC gain A_{d1} of this amplifier is approximated as

$$\begin{aligned} A_{d1} =& g_{m1} r_{out} \\ \approx& g_{m1}[(g_{m3} r_{o3}[r_{o1} \parallel r_{o2}] \parallel (g_{m4} r_{o4} r_{o5})] \end{aligned} \tag{6}$$

where g_{m3} and g_{m4} are the transconductance of the transistors M_{3b} and T_{4b}, and r_{o1}, r_{o2}, r_{o3}, r_{o4} and r_{o5} are the drain–source resistances of transistors M_{1b}, M_{2b}, T_{3b}, M_{4b} and M_{5b}.

Assuming the load impedance is parallel with R_L, C_L, Fig. 9, and $R_1, R_2 \gg R_L$, $r_{o6} \gg R_L$, the DC gain A_d at the regulator output is approximated as

$$\begin{aligned} A_d =& \frac{V_{PWR}}{V_i} \\ =& A_{d1} g_{m6}[r_{o6} \parallel (R_1 + R_2) \parallel R_L] \\ \approx& A_{d1} g_{m6} R_L \\ \approx& g_{m1}[(g_{m3} r_{o3} r_{o2} \parallel (g_{m4} r_{o4} r_{o5})] g_{m6} R_L \end{aligned} \tag{7}$$

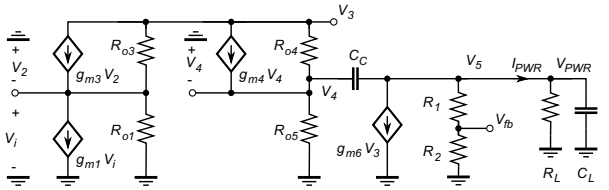

Figure 9. Schematic diagram of the regulator open loop simplified small signal equivalent network.

where g_{m6} is the transconductance of the M_6 transistor and r_{o6} is its drain–source resistance. The open loop gain A_{op} relative to the node V_{fb} is

$$\begin{aligned} A_{op} =& \frac{V_{fb}}{V_{in}} = A_d \beta \approx A_{d1} g_{m6} R_L \frac{R_2}{R_1 + R_2} \\ \approx& g_{m1}[(g_{m3} r_{o3} r_{o2} \parallel (g_{m4} r_{o4} r_{o5})] g_{m6} R_L \end{aligned} \tag{8}$$

where $\beta \approx 0.5$ is the loop feedback factor.

In the analysis of the open loop transfer function, for simplicity, we ignore the body effects, assume that the amplifier is symmetric, and the output impedance of the PMOS mirror $M_{2a,b}$ is very large, which leads into the open loop equivalent half–circuit model network, Fig. 9, with the folded–cascode amplifier.

Using KCL, and after solving for the internal voltage V_2, V_3, V_4 it is possible to derive the transfer function $H(s)$ of the regulator open loop as

$$\begin{aligned} H(s) =& \frac{V_{PWR}}{V_i} \\ =& \frac{A_{d1} A_{d2} \left(1 + \dfrac{s}{G4/C_c}\right)}{(1 + s C_c g_{m6} R_L R_{out3}) \left(1 + \dfrac{s C_L}{g_{m6} G_2 r_{o4}}\right)} \end{aligned} \tag{9}$$

where,

$$\begin{aligned} R_{out3} \approx& \frac{(g_{m4} r_{o4} r_{o5} + r_{o4} + r_{o5})(g_{m3} r_{o1} r_{o3} + r_{o1} + r_{o3})}{(g_{m4} r_{o4} r_{o5} + r_{o4} + r_{o5}) + (g_{m3} r_{o1} r_{o3} + r_{o1} + r_{o3})} \\ A_{d1} =& g_{m1} R_{out3} \\ A_{d2} =& g_{m6} R_L \end{aligned}$$

Hence, the loop transfer function has one zero, ω_z, and two poles, ω_{p1} and ω_{p2},

$$\omega_z = \frac{G_4}{C_c} = \frac{g_{m4} + g_{o4} + g_{o5}}{C_c} \tag{10}$$

$$\omega_{p1} = \frac{1}{R_{out3} A_{d2} C_c} \tag{11}$$

$$\omega_{p2} = \frac{g_{m6}}{C_L} \tag{12}$$

As $\omega_{p2}, \omega_z \gg \omega_{p1}$, the unity gain bandwidth, ω_0 is set by $|H(s)| = 1$ as

$$\omega_0 = \frac{g_{m1}}{C_c} \tag{13}$$

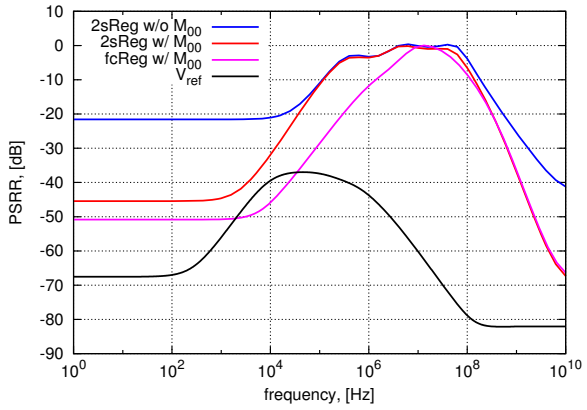

Figure 10. Simulated graphs for PSRR of V_{PWR} vs. frequency of the closed loop regulator driving a load ($R_L = 250\Omega$): using a two–stage classical amplifier without M_{00} transistor (2sReg w/o M_{00}); using a two–stage classical amplifier with M_{00} transistor (2sReg w/ M_{00}); using folded–cascoded amplifier with M_{00} transistor (fcReg w/ M_{00}); and PSRR of the voltage reference itself (V_{ref}), (Typical process, $T = 37\,^{\circ}C$, $V_{PWR} = 1.0V$).

The phase margin of this loop is approximated as

$$\begin{aligned} PM \approx & 180 + \tan^{-1}\frac{\omega_0}{\omega_z} - \tan^{-1}\frac{\omega_0}{\omega_{p1}} - \tan^{-1}\frac{\omega_0}{\omega_{p2}} \\ = & 180 + \tan^{-1}\frac{g_{m1}}{g_{m4} + g_{o4} + g_{o5}} \\ & - \tan^{-1}(g_{m1} R_{out3} A_{d2}) \\ & - \tan^{-1}\frac{g_{m1} C_L}{g_{m6} C_c} \end{aligned} \tag{14}$$

and as expected it is controlled, aside from g_m values of the input and output stages, by the values of the loading and compensation capacitances.

A. Power supply rejection ratio (PSRR)

One of the main design goals of this design is to minimize circuit sensitivity to the variations of the available voltage levels. In order to quantify available choices and decide what compromises to make, we studied and compared performance of three different configurations of our regulator, one with folded–cascode amplifier with the M_{00} transistor ('fcReg w/ M_{00}'), and one with a traditional two–stage amplifier (schematic not shown) in combination both with ('2sReg w/ M_{00}') and without ('2sReg w/o M_{00}') the M_{00} transistor, Fig. 10.

The simulations show that, in terms of PSRR, the regulator based on folded–cascode amplifier with the M_{00} relative to the 2–stage amplifier exhibits approximately $6dB$ better PSRR in the LF range (i.e. $-45dB$ vs. $-51dB$), which increases to $15dB$ in the mid–band, and becomes similar in the HF band. However, at DC, the regulator using the 2–stage amplifier exhibits better line and load regulation (Table I), which is attributed to the slightly bigger systematic input offset ($0.2mV$ to $0.8mV$) in the cascoded amplifier. In both cases, the PSRR is dominated by M_{00} which improves the PSRR. At the same time, the bandgap voltage reference by itself exhibits $-68dB$ PSRR at LF and over $-80dB$ at HF, Table II. For comparative purposes and illustration of the compromises we reference the state of the art experimental work [11].

Table I
PERFORMANCE OF REGULATOR CIRCUIT

Parameters		Folded	Two–stage	[11]
CMOS Technology		130nm		$0.18\mu m$
Supply current (with bandgap)	$[\mu A]$	11.6	12.2	28
Drop voltage	[mV]	400	400	300
Regulator output	[V]	0.99	0.99	1.8
Line Regulation (full load)		0.31%	0.14%	0.024%
Load Regulation	[mV/4mA]	1.16	0.2	0.7
Settling time	$[\mu s]$	7.9	21	1.6
Stability Range		Full load	Full load	Full load
PSRR @1kHz		-51	-45	-70
@1GHz	[dB]	-36	-37	-
Compensation		845fF	8.46pF	-
Spot Noise @100Hz		1.8	1.73	1.1
@100kHz	$\left[\mu V/\sqrt{Hz}\right]$	312	325	390

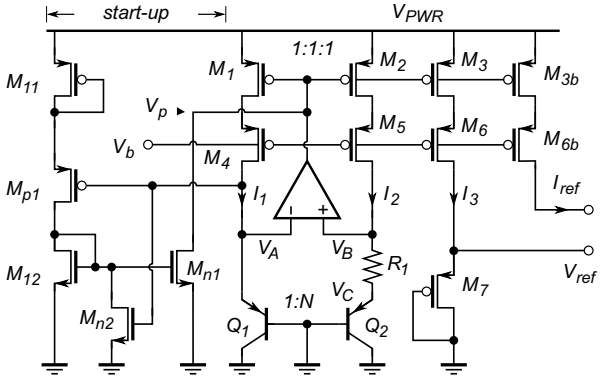

Figure 11. Simplified schematic diagram of on–chip voltage/current reference circuit that consists of PTAT core, V_{ref} generator, I_{ref} generator, and the start–up sections (biasing voltage V_b generator not shown).

IV. VOLTAGE AND CURRENT REFERENCE

Although the conventional expression for the gate–source voltage V_{GS} of a MOS transistor in saturation indicates that it is possible to make it temperature independent, alas only at one specific constant current biasing point I_{p0} (which may have relatively high current value), e.g. in the case of a PMOS transistor, at

$$|V_{GSp}| = |V_{tp}| + \sqrt{\frac{2I_p}{\mu_p C_{ox}(W/L)_p}} \tag{15}$$

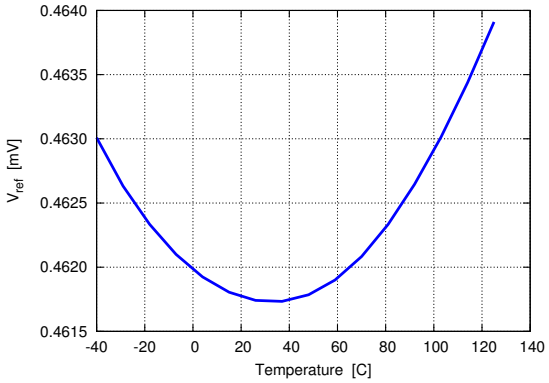

Figure 12. Simulated reference voltage V_{ref} over the full temperature range (TT, $V_{PWR} = 1.0V$) centred around the body temperature.

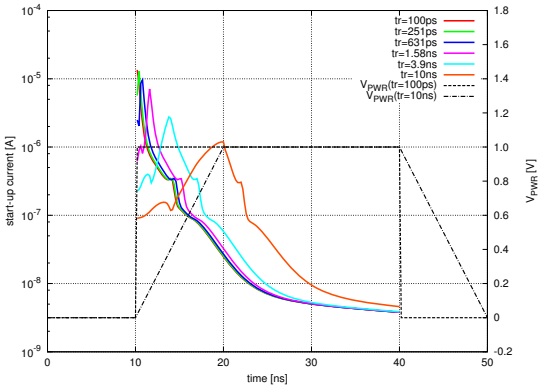

Figure 13. Simulated transient start–up currents vs. rise times of the bandgap power supply voltage V_{PWR} from $tr = 100ps$ to $tr = 10ns$. For the sake of providing the time reference, two pulses of the power supply voltage V_{PWR}, one with $tr = 100ps$ and one with $tr = 10ns$, are also shown.

where $|V_{tp}|$ is the PMOS threshold voltage, μ_p is the carrier mobility, C_{ox} is the unit gate oxide capacitance, I_p is the bias current, and $(W/L)_p$ is the gate width to length ratio. Therefore, a temperature independent voltage/current reference is required.

Our bandgap voltage/current reference circuit consists three functional blocks, the proportional to absolute temperature (PTAT) voltage generator core, the reference voltage generation circuit, and the low–voltage start–up circuit, Fig. 11. The core generates PTAT current that is mirrored to the diode-connected PMOS M_7 so that its gate–source voltage V_{GSp} in (15) is temperature independent. Source current I_2 in the core PTAT circuit, Fig. 11, is given by (16), where the low–temperature coefficient resistor R_1 is made of p–polysilicon whose resistance changes from -0.5% to 1% over the full temperature range of $-40\,^{\circ}C$ to $125\,^{\circ}C$. For the additional improvement in PSRR, the PMOS cascode mirrors M_1–M_6 are employed.

The PTAT core amplifier, Fig. 11, works down to $0.9V$ supply and typically consumes $0.9\mu A$ current while providing more than $50dB$ DC gain. The high DC gain helps to suppress the amplifier offset voltage V_{os}, hence the PTAT current is

$$I_2 = \frac{\Delta V_{eb} + V_{os}}{R_1} = \frac{kT}{qR_1} \ln N + \frac{V_{os}}{R_1} \qquad (16)$$

where k is the Boltzman constant, T is the absolute temperature, q is the electron electrical charge, and N is the current density ratio of Q_1 and Q_2. For the case of $N = 8$, the base–emitter voltage difference $\Delta V_{EB} = V_B - V_C$ has a positive temperature coefficient of about $0.18mV/C$. The value of the resistor R_1 is then found from the temperature sensitivity of the second term in (15) as

$$\frac{\partial \sqrt{\frac{2I_p}{\mu_p C_{ox}(W/L)_p}}}{\partial T} = \frac{1}{g_{m7}} \frac{\partial I_p}{\partial T} - \sqrt{\frac{I_p}{2\mu_p^3 C_{ox}(W/L)_p}} \frac{\partial \mu_p}{\partial T} \qquad (17)$$

where g_{m7} is the transconductance of the diode-connected PMOS M_7. For a given W/L, the negative temperature sensitivity of the PMOS threshold voltage V_{tp}, which is about $-0.79mV/C$, is then cancelled with the positive temperature coefficient of (17), which is about $+0.39mV/C$ at $35\,^{\circ}C$ for the 2nd term. This leads to $R_1 = 56.5k\Omega$. As the absolute resistor value changes $\pm 15\%$ over the process, R_1 is implemented as a programmable array so that it can be trimmed as needed.

The temperature variation of the reference voltage is over the full temperature range is shown in Fig. 12. We keep in mind that for the implantable circuit applications, the environment temperature is very stable, i.e. at the body temperature, which means that optimization of PSRR is much more important and challenging task.

A. PTAT Start–up circuit

A low voltage start–up circuit, Fig. 11, is designed to provide the initial current to the PTAT during the powering up transition. The initial circuit condition is that bipolar transistors Q_1 and Q_2 have zero collector currents. Therefore nodes V_A and V_B are at ground level. Hence, the switch PMOS M_{p1} is on while the NMOS switch M_{n2} is off. The switch M_{p1} enables the voltage divider $M_{11,12}$, which turns on NMOS switch M_{n1}. Consequently, M_{n1} pulls the node V_p to ground and turns on the $M_{1,2,3,3b}$ PMOS mirrors. Because the cascoded devices in the current mirrors $M_{1,4}$–$M_{2,5}$ are biased from the supply rail they are turned on shortly after the power is up. Hence, the initial startup current is injected into Q_1 and Q_2, which progressively increases voltages at nodes V_A and V_B. At the end of the start–up process, voltage at V_A settles in the $0.5V$ to $0.8V$ range within the full temperature range. Subsequently, M_{n2} turns on, which is followed by the potential at the M_{n1} gate being pulled to the ground. Hence, the start–up circuit

Table II
PERFORMANCE OF THE BANDGAP REFERENCE CIRCUIT

Parameter		This work	[12]	[13]	[14]	[15]
CMOS Technology		130nm		$0.6\mu m$		$0.18\mu m$
Minimum power supply	[V]	0.9	1	1.4 to 3	0.98V	1V
Power supply current	$[\mu A]$	4	26	9.7	18	29.5
Output voltage	[V]	0.462	0.798	0.309	0.603	0.7395
Temperature coefficient (sim.)	$[ppm/^\circ C]$	24.74	-	-	-	1.18
Temperature coefficient (meas.)	[ppm/$^\circ C$]	-	6.64	36.9	15(trim)	-
Temperature range	$[^\circ C]$	-40 to 125	-50 to 160	0 to 100	0 to 100	-30 to 130
Line regulation	$[ppm/V]$	90.4	248	830	4230	850
Power Supply Gain @ 10Hz	[dB]	-68	-58	-47	-44	-52
Spot Noise @ (1kHz)	$\left[nV/\sqrt{Hz}\right]$	418	-	-	-	-
Spot Noise @ (100kHz)	$\left[nV/\sqrt{Hz}\right]$	34	-	1.6	-	-
Output Load		50pF	-	100nF	-	

is disconnected from the PTAT circuit. Soon after voltage V_A settles high enough, M_{p1} is turned off and therefore it breaks the DC current path in the voltage divider. By using Monte–Carlo analysis we confirmed that this strategy works well under wide voltage supply, process corners and the environment variations.

Examples of simulation transients behaviour of the start–up circuit, Fig. 13, demonstrate that the start–up current drops down to a couple of nano–amperes (i.e. the leakage current) within 20ns after the power is turned on.

B. The Regulator Circuit Simulations

Temperature variations inside a living body are very small and centred at approximately $37\,^\circ C$, therefore a satisfactory voltage reference is achieved without any additional compensation. The temperature dependance curve is tuned to have its minimum at the body temperature with $24.74ppm/C$ variation, Fig. 12. At $37\,^\circ C$, the complete circuit including the amplifier, draws $4.0\mu A$ current from the $0.9V$ supply. To the best of our knowledge, this is the lowest reported power in standard CMOS implementation. Voltage V_{ref} is stable in the ($V_{dd} = 0.9V$ to $1.5V$) range with the power supply sensitivity of $90.4ppm/V$. The reference voltage frequency response curve, Fig. 10, shows that PSRR is $-68dB@10Hz$ and $-82dB@1GHz$. Comparative performance of the temperature insensitive voltage reference is summarized in the Table II, and we make reference relative to experimental works [12] to [15].

The complete regulator circuit is simulated with range of loading impedances, and the simulation confirmed that in the worst case scenario, the fully–loaded regulated supply with folded–cascode amplifier, the reference voltage V_{ref} is stable for voltage supply in the range of 1.3V to 1.9V with a power supply sensitivity of $2.97ppm/V$. For moderate to low impedance loads, the reference operates with supply voltages as low as $0.9V$, while the regulated power supply voltage may be as low as $1V$, Fig. 14.

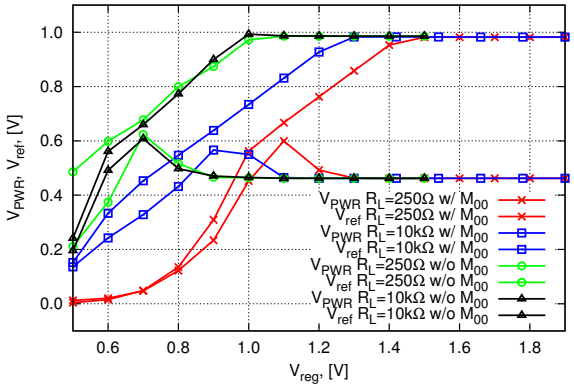

Figure 14. Simulated output of the reference and regulator (using folded–cascode amplifier) voltages versus variation of the supply voltage (full load).

V. SUMMARY

We presented a 130nm CMOS design architecture of a low–power voltage regulator suitable for EM energy scavenging front end in implantable circuits. The reference circuit has a typical $24.74ppm/\,^\circ C$ and maximum $45ppm/\,^\circ C$ temperature sensitivity over the combinations of process, temperature and power supply. The voltage reference circuit by itself consumes $3.6\mu W$ with the line regulation of $90.4ppm/V$. A novel start–up circuit suitable for low–voltage application is also proposed. The overall circuit, including the reference bias, error amplifier and the feedback network, consumes $18\mu W$ typically. The low power consumption and low supply voltage make this block suitable for the implantable medical telemetry system application.

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