# Analysis of Multistage Sampling Rate Conversion for Potential Optimal Factorization

Zhengmao Ye, Habib Mohamadian
Southern University, Baton Rouge, Louisiana, USA
Email: zhengmao_ye@subr.edu, habib_mohamadian@subr.edu

*Abstract* — **Digital multistage sampling rate conversion has many engineering applications in fields of signal and image processing, which is to adapt the sampling rates to the flows of diverse audio and video signals. The FIR (Finite Impulse Response) polyphase sampling rate converter is one of typical schemes that are suitable for interpolation or decimation by an integer factor. It also guarantees the stability performance with the stable gain margin and phase margin. The big challenge occurs upon implementation when a very high order filter is needed with large values of L (positive integer factor of interpolator) and/or M (positive integer factor of decimator). Narrowband linear phase filter specifications are hard to achieve, however. It leads to extra storage space, additional computation expense and detrimental finite word length effects. The multistage sampling rate converter has been introduced to factorize the L and M ratio into a product of ratios of integers or prime numbers. The optimal number of stages and optimal converting factors are both critical terms to minimize the computation time and storage requirements. Filter structure analysis is conducted in this study to search for the potential factors that could have a remarkable impact to optimize the sampling rate conversion.**

***Keywords- Polyphase FIR Filter, Interpolation, Decimation, Sampling Rate Conversion, Multistage, Multirate, Optimization***

## I. INTRODUCTION

The sampling process stems from obtaining discrete time signals from the continuous time signals at the regular time intervals. Sampling can be conducted for functions varying in space, time, or any other dimension. For discrete time signals, potential upsampling, downsampling and multirate multi-stage sampling rate conversion can be applied as well [1-2]. There are a wide variety of important real world applications on sampling. For instance, the emerging GPS (Global Positioning System) enabled cell phones offer new opportunities of data collection in the massive volumes at relatively cheaper cost than the dedicated probe vehicles. The traffic monitoring applications need to firstly determine whether the GPS-enabled cell phone is actually in an automobile and secondly, it needs to match the current GPS device location to a corresponding link on a GIS (Geographic Information System) map. A methodology is developed to determine relationships between the cell phone pinging sampling rate and accuracy of mode detection and map matching processes. It is found that the higher the number of pings per interval and the longer the data trace interval, the better the accuracy. The impact of the sampling frequency on the map matching algorithm is found to be a function of link length, current speed of a vehicle and period of the day [3]. In many cases, sampling rate conversion is required by digital systems dedicated to audio and speech processing in order to adapt the sample rate to different signal flows. For example, 8 kHz and 16 kHz for speech, 32 kHz for broadcasting, 44.1 kHz for CDs, and 48 kHz for studio work. The sampling rate conversion (SRC) is based on the objective criteria, such as complexity, integration cycle and performance characterization. The proposed SRC system has the capability of fully recovering characteristics and rounding noise behavior [4]. A linear phase Finite Impulse Response (FIR) filter of an arbitrary order is designed for the sampling-rate conversion by a rational factor of L/M (upsampling / downsampling) also. The coefficient symmetry of the linear-phase filter is exploited with a minimal number of delay elements. The number of multiplications per output sample is reduced approximately by a factor of two compared with the conventional polyphase implementation [5]. Similarly, a class of farrow-structure-based reconfigurable bandpass FIR filters for integer sampling rate conversion is introduced. Both Mth-band and general FIR filters can be realized and the filters work equally well for any integer factor and passband location. The proposed sampling rate converters provide the considerably higher efficiency and fewer filter coefficients [7]. Rational sampling rate conversion can also be performed in the domains of discrete Fourier transform and discrete cosine transform. Conversion error performance and computational complexity are based on the proposed fast transform algorithms. It can achieve substantial improvements on the conversion accuracy at the reduced computational cost, compared with the conventional lowpass filter [6]. To evaluate the performance of sampling receiver, a sub-Nyquist rate sampling receiver architecture is presented that exploits signal sparsity by employing compressive sensing techniques. The receiver works at sampling rates much lower than the Nyquist rate whose performance is quantified analytically. A new parallel path structure is used. The receiver performance is quantified analytically. It is shown that an instantaneous receiver signal bandwidth of 1.5 GHz and a Signal to Interference plus Noise Ratio (SINR) of 44 dB are achievable [8]. Upsampling and downsampling can further be applied to digital image processing to enhance the image quality [9-10].

From the most recent research outcomes, the problem of optimal multistage sampling rate converters has never been solved in terms of both the optimal number of stages and the optimal converting factor. For concern of the potential optimal solution, a case study has been made based on an example of the cascades of FIR polyphase filter design when converting the sampling rate for a stream of signals from audio DVD data (96 kHz) to audio CD data (44.1 kHz) with some interesting new results.

## II. Single Stage Sample Rate Conversion

In order to convert a stream of signals from 96 kHz to 44.1 kHz, the FIR lowpass filter structure is selected to perform the single stage sampling rate conversion. By nature, in contrast to the Infinite Impulse Response (IIR) filter, FIR filters are always stable and easy to implement with all poles located at the origin. On the other hand, a higher order is necessary. For a matter of simplicity, upsampling and downsampling are processed in the single stage, where anti-aliasing filtering is applied before downsampling (decimation) and anti-imaging filtering is applied after upsampling (interpolation). The combined cutoff frequency is selected as the minima of anti-aliasing filtering and anti-imaging filtering. The frequency response of the single stage sampling rate conversion is shown in Fig. 1. Due to the large values of L (147) and M (320), a narrowband lowpass FIR filter has been produced. It is tough to implement while a very high order filter is necessary. The finite word length effect is thus generated. Also extra storage space and long simulation time are needed. The multistage sampling rate converter is an alternative to the single stage sampling rate converter. The multistage structure serves as a tradeoff to the harmful finite word length effects. The conversion ratio can be translated into a product of ratios, where smaller factorized values of the interpolation factor (L) and decimation factor (M) will be achieved. From literatures there is no systematic approach in determining an optimal number of stages and an optimal structure to factorize a set of L/M ratio so as to minimize the computation time and storage space. The trial and error method is mostly applied so far.

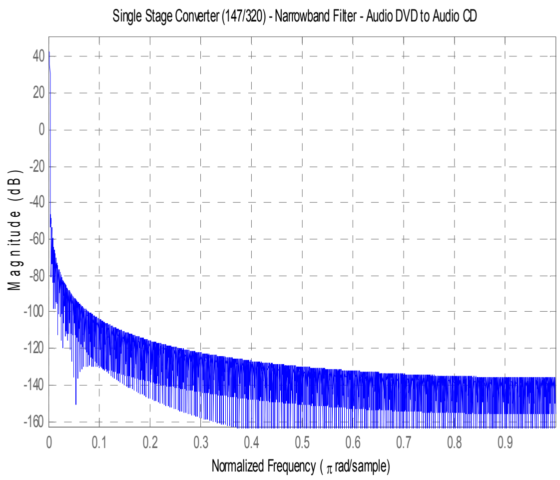


**Fig. 1 Single Stage Sampling Rate Conversion - Narrowband Filter**

## III. MultiStage Sample Rate Conversion

The multistage sampling rate converter has been designed to substitute the single stage sample rate conversion. Overall it is a downsampling process (decimation) and three stage cascade structure has been applied. The block diagram is shown in Fig. 2, where three composite anti-aliasing and anti-imaging filters H1(f), H2(f) and H3(f) are applied to each stage, respectively.

**Fig. 2 Multiple Stage Sampling Rate Conversion**

Since the three stage factorization approaches for the required L/M ratio of 147/320 are not unique, three typical cases are chosen whose filter specifications are shown in Table 1. Here, the stage conversion rates of three cases have been selected as:

A. [7, 7, 3] / [8, 5, 8]
B. [7, 3, 7] / [8, 5, 8]
C. [7, 3, 7] / [8, 4, 10]

where a combination of two decimators and one interpolator is applied in Case A, while combinations of three adjustable decimators are applied in Case B and Case C. At each stage of all 3 cases, the ideal gains of the low frequency passbands, sampling rates and cutoff frequencies are also provided.

**Table 1. Specifications for Multiple Stage Converter Design**

| Sample Rate Conversion 96 to 44.1K | L/M | H(f) Passband | fs (kHz) | F (kHz) | Order |
|---|---|---|---|---|---|
| Single Stage | 147/320 | | | | 7680 |
| **A - Stage 1** | **7/8** | **7** | **96** | **6** | **192** |
| A - Stage 2 | 7/5 | 7 | 84 | 6 | 168 |
| A - Stage 3 | 3/8 | 3 | 117.6 | 7.35 | 192 |
| **B - Stage 1** | **7/8** | **7** | **96** | **6** | **192** |
| B - Stage 2 | 3/5 | 3 | 84 | 8.4 | 120 |
| B - Stage 3 | 7/8 | 7 | 50.4 | 3.15 | 192 |
| **C - Stage 1** | **7/8** | **7** | **96** | **6** | **192** |
| C - Stage 2 | 3/4 | 3 | 84 | 10.5 | 96 |
| C - Stage 3 | 7/10 | 7 | 63 | 3.15 | 240 |

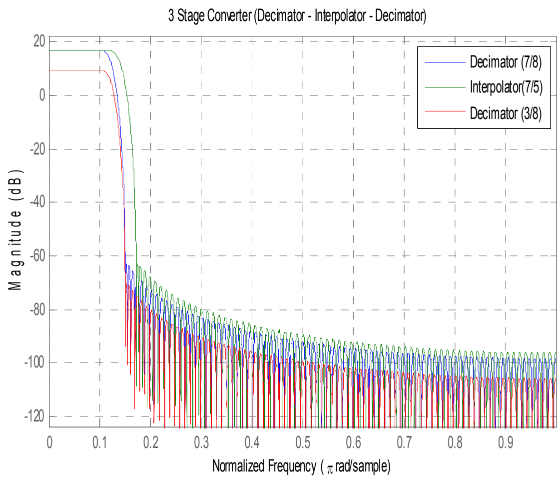


**Fig. 3 Three Stage Sampling Rate Conversion – Case A**

In addition, small integer factors are the solutions with the low fractional rate conversions in each case. Thus the FIR polyphase sample rate converters are applied to decimator and interpolator design. The reason is that the polyphase FIR filters are well suitable for interpolation or decimation by a small integer factor. In this way, detrimental finite word length effects can be avoided. The regular lowpass filters can be formulated in this way rather than the single stage narrowband lowpass filter. It can be shown in Table 1 that the orders of three stage sampling rate converters are much lower than that of the single sampling rate converters (i.e., 7680). Using the multistage approach, an audio DVD to audio CD converter can be realized. The frequency responses of the multirate three stage sampling rate converters are plotted in Figs. 3-5. At the same time, among three different cases, case A has a relatively higher order design than Case B and Case C.

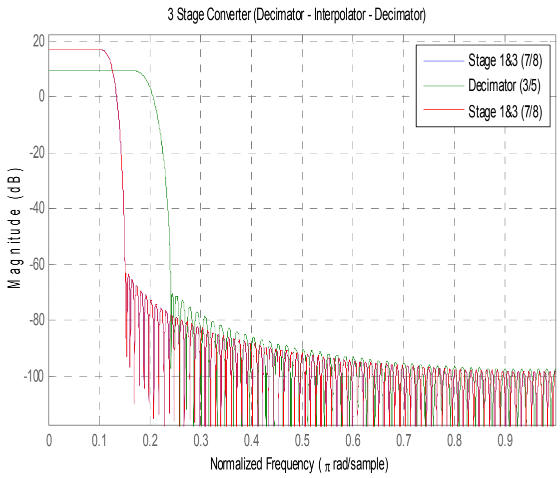


**Fig. 4 Three Stage Sampling Rate Conversion – Case B**

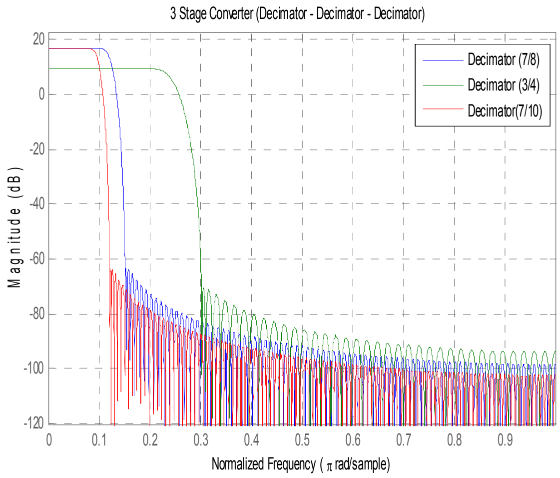


**Fig. 5 Three Stage Sampling Rate Conversion – Case C**

## IV. DETAILED CASE STUDIES VIA BODE PLOT

The Nyquist–Shannon sampling theorem is strictly followed upon the design of direct-form FIR polyphase sampling rate converter. Hence, the source signals can also be reconstructed as the bandwidth of a baseband signal is less than the Nyquist frequency. The right choice of the FIR structure ensures the stability of filter design. This fact is also clearly shown in the Bode diagrams as Figs. 6-8, where the stable gain margin and phase margin have been depicted in all cases, no matter it is a higher order filter or lower order FIR filter. Essentially, this sampling rate converter is a decimator instead of an interpolator. Therefore, as Case A has a separate stage of the interpolator design, it results in a relatively higher order design than two other cases with the cascade structure of three decimators. For Case B and Case C, further analysis is needed to compare the merit and drawback.

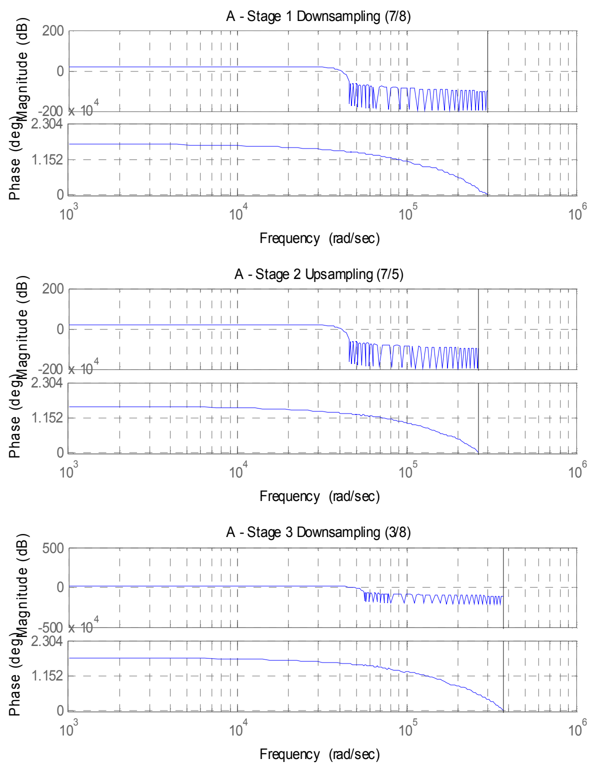


**Fig. 6 Bode Plot of Multistage Interpolator and 2 Decimators – Case A**

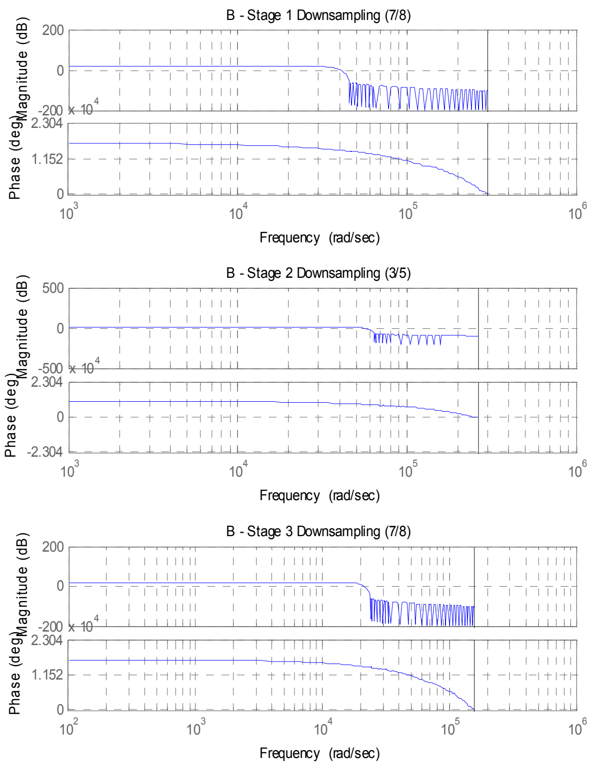


**Fig. 7 Bode Plot of 3 Multistage Decimators – Case B**

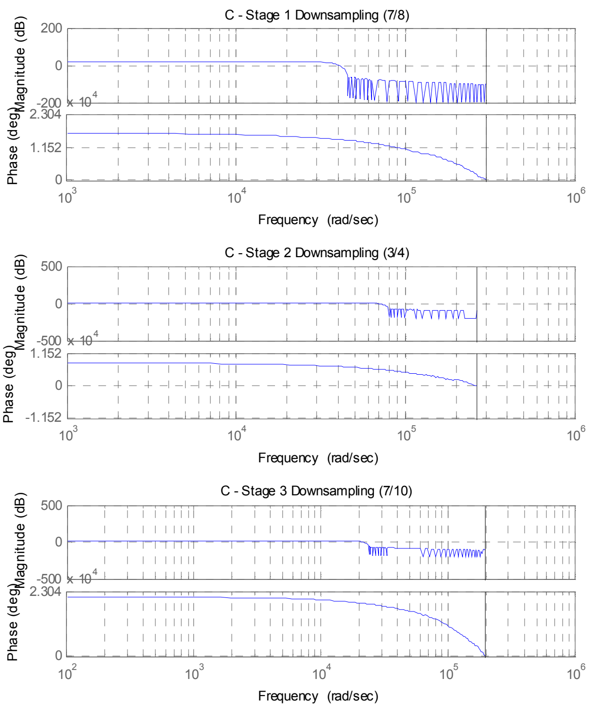


**Fig. 8 Bode Plot of 3 Multistage Decimators – Case C**

## V. COMPLEXITY IN MULTISTAGE CONVERTER DESIGN

To quantify the storage space and computation time needed for sampling rate conversion, a simple way could be achieved by comparing the actual amount of adders and multipliers being used as well as the number of states associated. For the high order single stage sampling rate converter and three low order multistage sampling rate converters being employed, the related expenses are listed in Table 2. Among 3 individual cases, when all three stages are counted together, Case A requires maximal numbers of states and electronic elements since a single stage interpolator has a negative effect on the overall decimator design. Case B requires a similar number of states to Case C but it requires less numbers of adders and multipliers than Case C. It results from the fact that more prime number factors of interpolation and decimation are used in Case B than Case C.

**Table 2. Expense for Sampling Rate Converter Design**

| Expense (Quantity) | States | Adder | Multiplier | Adder + Multiplier |
|---|---|---|---|---|
| Single Stage | 52 | 7510 | 7657 | 15167 |
| A - Stage 1 | 27 | 162 | 169 | 331 |
| A - Stage 2 | 23 | 138 | 144 | 282 |
| A - Stage 3 | 63 | 166 | 169 | 335 |
| B - Stage 1 | 27 | 162 | 169 | 331 |
| B - Stage 2 | 38 | 94 | 97 | 191 |
| B - Stage 3 | 27 | 162 | 169 | 331 |
| C - Stage 1 | 27 | 162 | 169 | 331 |
| C - Stage 2 | 31 | 70 | 73 | 143 |
| C - Stage 3 | 34 | 210 | 217 | 427 |

## CONCLUSIONS

Diverse types of data in the forms of audio, video or radio frequency signals are preferably processed in the digital domain. The conversion among different types of signals is frequently applied. Single stage sampling rate conversion is straightforward but the high order requirement represents a big challenge. The multistage sampling rate converter is a better solution. It is however still subject to optimization. There is no existing solid rule to reach the optimal number of stages and the optimal factor of L/M for the concern of computation time and memory storage. Case studies have been conducted in this article to seek for some feasible means towards the best solution of sampling rate conversion. If possible, each stage of multistage converters should be selected following the actual type of the single stage converter exactly, either decimator or interpolator. Also the prime number factors for interpolation and decimation are preferable throughout the upsampling and downsampling processes.

## REFERENCES

[1] R.Schilling, S.Harris, “Fundamental of Digital Signal Processing using MATLAB”, Cengage Learning, 2nd Edition, Cengage Learning, 2012

[2] Vinay K. Ingle, John G. Proakis, "Digital Signal Processing", 2nd Edition, Cengage Learning, 2007

[3] Y. Byon, B. Abdulhai, A. Shalaby, “Impact of Sampling Rate of GPS-Enabled Cell Phones on Mode Detection and GIS Map Matching Performance”, 2007 Transportation Research Board 86th Annual Meeting, Washington DC, Jan 21-25, United States

[4] S. Tassart, "Time-invariant context for sampling rate conversion systems", IEEE Transactions on Signal Processing, v 60, n 3, p 1098-1107, March 2012

[5] R. Bregovic, Y. Yu, T. Saramaki, C. Yong, "Implementation of linear-phase FIR filters for a rational sampling-rate conversion utilizing the coefficient symmetry", IEEE Transactions on Circuits and Systems, v 58, n 3, p 548-561, 2011

[6] G. Bi, S. Mitra, S. Li, "Sampling rate conversion based on DFT and DCT", Signal Processing, v 93, n 2, p 476-486, Feb. 2013

[7] H. Johansson, "Farrow-structure-based reconfigurable bandpass linear-phase FIR filters for integer sampling rate conversion", IEEE Transactions on Circuits and Systems II: Express Briefs, v 58, n 1, p 46-50, January 2011

[8] X. Chen, Z. Yu, S. Hoyos, B. Sadler, "A Sub-Nyquist Rate Sampling Receiver Exploiting Compressive Sensing", IEEE Transactions on Circuits and Systems, v 58, n 3, p 507-520, March 2011

[9] R. Gonzalez, R. Woods, “Digital Image Processing,” 3rd Edition, Prentice-Hall, 2007

[10] Z. Ye, H. Mohamadian and Y. Ye, "Information Measures for Biometric Identification via 2D Discrete Wavelet Transform", Proceedings of 2007 IEEE International Conference on Automation Science and Engineering (CASE 2007), pp. 835-840, Sept. 22-25, 2007, Scottsdale, Arizona, USA