Trend of High-Speed SAR ADC towards RF Sampling

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ABSTRACT

One emerging trend of high-speed low-power ADC design is to leverage the successive approximation (SAR) topology. It has successfully advanced the power efficiency by orders of magnitude over the past decade. Given the nature of SAR algorithm, the conversion speed is intrinsically slow compared to other high-speed ADC architectures, and yet minimal static power is required due to the mostly digital implementation. This paper examines various speed enhancement techniques that enable SAR ADCs towards RF sampling, i.e. >GS/s sampling rate with >GHz input bandwidth, while maintaining low power and area consumption. It is expected to play a crucial role in the future energy-constrained wideband system.

I. INTRODUCTION

High-speed medium-resolution ADCs are widely adopted by electronic systems, such as instrumentations, disk read channel, high-speed serial links, optical communications, and wideband radios, etc. The ADCs in this category were initially dominated by Flash architecture with bipolar devices [1-5] in the 80s and early 90s due to the higher device speed. The first dramatic shift of paradigm began when the pervasive penetration of CMOS technology started in the late 90s. Despite that the device speed was not as high as bipolar devices, its low cost, wide adoption by digital and progressively improved speed have finally made high-speed CMOS ADC into reality [6-10]. From the architecture perspective, the Flash topology is preferred for high-speed operation since all the comparisons are accomplished within one clock cycle; however, the complexity increases exponentially with ADC resolution. It thus triggered other architectural possibilities in this realm, such as pipelined ADC architecture with time-interleaving [7, 11-15]. In the recent years, there is another major architectural shift towards high-speed SAR operation. Since the SAR architecture does not require linear analog amplification, it benefits more from the technology scaling. Much research has been engaged to push this power efficient architecture into high speed sampling regime, while it was conventionally limited to lower speed range, i.e. KS/s to MS/s, as illustrated in Fig. 1.

To prove the outstanding power efficiency of SAR architecture in relation to other ADC topologies, the performance of recent state-of-the-art high-speed ADCs is plotted in Fig. 2. The circled dots are the published ADC literatures based on SAR within the past decade, which indicate that the power efficiency has improved by orders of magnitude, particularly for the medium resolution high-speed operation up to tens GS/s sampling rate.

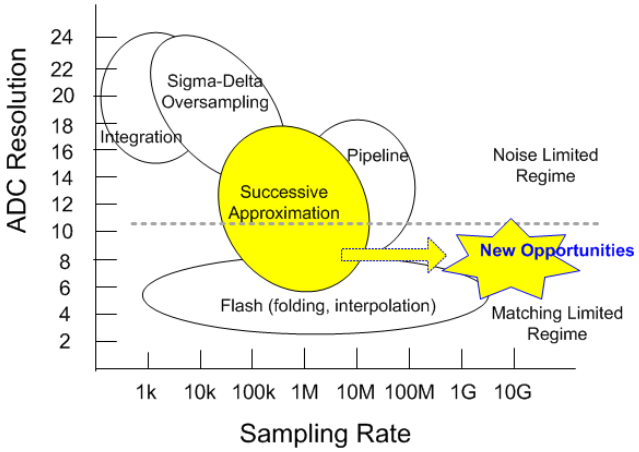

Figure 1 Emerging paradigm shift by leveraging SAR architecture

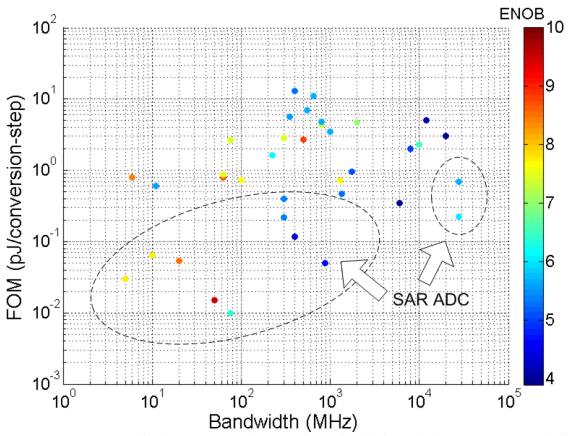

Figure 2 Power efficiency vs. input bandwidth of the recent published Nyquist ADCs

This paper overviews various critical techniques to enable this level of high-speed and low-power operation. An asynchronous SAR architecture will be described in section II, which effectively reduces the internal comparison time and complexity. Section III outlines a multi-bit per conversion cycle technique that reduces the required number of SAR comparison cycles. Pipelined (section IV) and time interleaved (section V) SAR further increases the sampling rate through pipelining multiple conversion stages or parallelizing an array of SAR ADCs. The paper will be concluded in section VI.

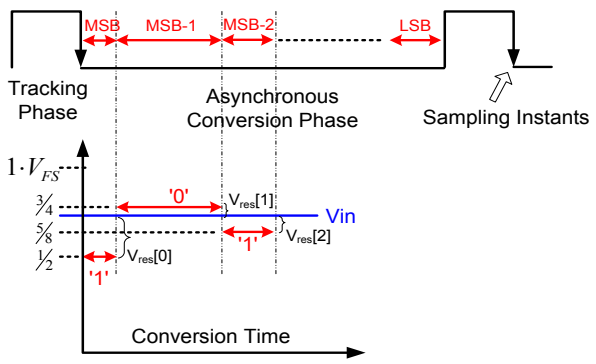

Figure 3 Concept of asynchronous SAR conversion

II. ASYNCHRONOUS SAR

The concept of asynchronous SAR architecture was first introduced in [16]. It aims to eliminate the conversion speed constraint of a conventional synchronous SAR ADC, which relies on an internal clock to divide the time into signal tracking and individual bit comparison phase from MSB to LSB. Since every clock cycle must tolerate the worst-case comparison time as well as the clock jitter, the overall conversion speed is constrained by design. The key idea of asynchronous SAR is to trigger the internal comparison from MSB to LSB like dominoes. Whenever the current comparison is complete, a ready signal is generated and triggers the following comparison immediately. The reduction in the overall comparison time is thus achieved due to the time savings in those faster conversion cycles, as shown in Fig. 3. Moreover, no high speed internal clock is needed, which leads to a low complexity implementation. Note that, a global clock running at the sampling rate is still required to perform uniform sampling.

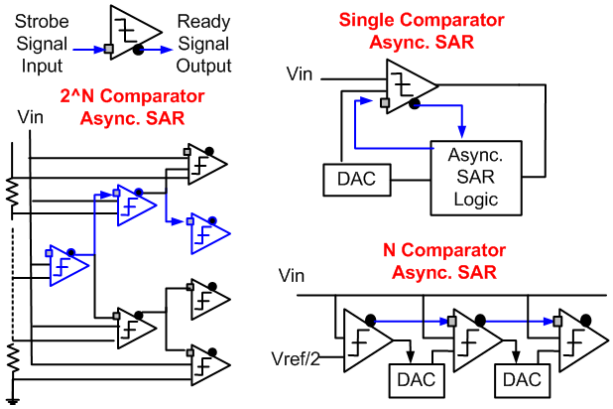

Figure 4 Potential implementations of asynchronous SAR

In terms of implementation, there are several variations to carry out the same asynchronous SAR algorithm including single, N and 2^N comparator configurations, as shown in Fig. 4. The single comparator configuration [16-18] consumes the least power and area among the three. However, if higher conversion speed is desired, the N or 2^N comparator configuration can be utilized to eliminate or reduce the time required for comparator reset and DAC settling [19, 20]. Note that, besides the additional hardware complexity, the offset voltage between the various comparators will degrade the ADC performance and hence extra calibrations are typically applied in the multi-comparator configurations.

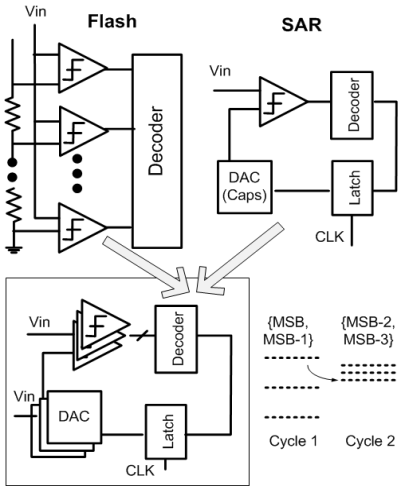

Figure 5 Multi-bit per cycle SAR architecture

III. MULTI-BIT PER CYCLE

Conventional SAR algorithm utilizes one comparison per cycle and hence requires at least N comparison cycles for an N-bit resolution. If more comparisons can be accomplished within one comparison cycle, the conversion time will be reduced proportionally, i.e. halved for 2bit/cycle case. Essentially, it is the combination of Flash and SAR ADC topology that are compromised in between the hardware complexity and sampling speed. The idea can be traced at least back to 60s' [21-23], where multiple reference DACs are built so that two bits are generated per cycle. In recent years, multiple capacitive DACs are utilized to sample the analog input and perform 2bit/cycle SAR algorithm by generating various reference levels [24]. To mitigate the drawback of additional capacitive loading, interpolation technique can be adopted with the mixture of resistive and capacitive DACs [25, 26]. The sampling speed of a single 2b/cycle SAR ADC has been demonstrated close-to 1GS/s with 6-8 bit resolution. Note that, the consequence of adopting such a Flash-like architecture is the vulnerability to the comparator offset, which leads to ADC nonlinearity. On the contrary, the comparator offset of a conventional 1b/cycle SAR only leads to the global offset without distortion. Therefore, the multi-bit per cycle SAR architecture is not as power efficient and most likely requires offset cancellation techniques. Another variation of a multi-bit per cycle SAR ADC is to utilize both voltage and time quantization that effectively provides multi-bit comparisons [27, 28]. It makes use of the input dependent delay of the comparator resolving time and allows SAR conversion to reduce switching activity and required conversion time.

IV. PIPELINING

Another common technique to improve the sampling speed is through pipelined conversion stages. Conventional pipelined ADC utilizes low resolution Flash ADC in each pipelined stage. The concept of pipelined SAR architecture is to replace the complex Flash ADC with power efficient SAR topology. As a result, one can allocate more quantization levels for each pipelined stage without much power penalty. Moreover, in the case of charge redistribution SAR ADC, the residue voltage is readily available on the capacitor network in the end of SAR

conversion, which can be re-used as part of the switch-capacitor residue amplifier [29, 30]. The architecture can also be extended to other low-power residue amplification techniques, such as an amplifier that dynamically charges up the second stage sampling capacitance depending on the residue voltage from the previous stage [19]. The drawback is the less accurate amplification and vulnerability to PVT variations which requires extra calibrations.

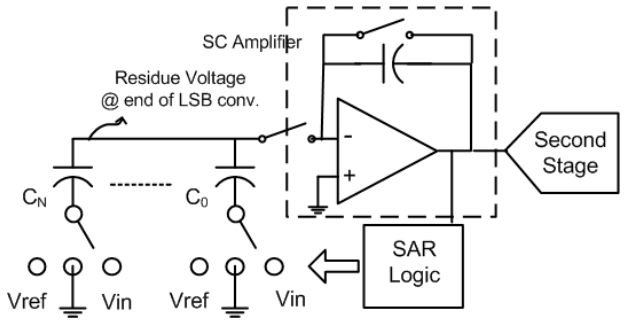

Figure 6 One embodiment of pipelined SAR

V. TIME INTERLEAVING

In the early 2000s, SAR ADC began its footprint in the high speed sampling regime (>hundreds MS/s) instead of operating in high resolution and lower sampling rate. In [31], it demonstrated that a 6bit, 600MS/s ADC is achievable via 8-way time interleaved SAR in 90nm CMOS with low power consumption. Ever since, the number of time interleaved SAR has been increasing consistently and a recent 8-bit, 56GS/s ADC was reported in [32] that consists of unprecedented 320-way 175MS/s SAR ADCs in 65nm CMOS. The ultra-high-speed ADC design has become somewhat similar to digital VLSI design, where massive parallelism is adopted for speed improvement. However, there are significant overheads associated massive time interleaved ADCs, including the capacitive loading of the sample-and-hold network, clock distributions, and mismatches in between the single ADCs. In this sub-section, several design techniques to alleviate these constraints will be reviewed.

First of all, the value of sampling capacitor should be minimized while maintaining sufficient matching accuracy. As more ADCs are time interleaved, the more sampling capacitors will load the previous driver stage and limit the achievable bandwidth. For example, if the tracking time is half of the entire sampling period, the driver of an M-way time interleaved ADC will be loaded with M/2 sampling capacitor at any given time. One way to alleviate the sampling capacitor loading issue is to divide the sampling switches into two stages. The first-stage front end sampling switches operate at a higher speed but with less capacitor loading [33]. However, the buffers in between the stages can become the linearity bottleneck. Another common approach is to reduce the tracking time so that only one sampling

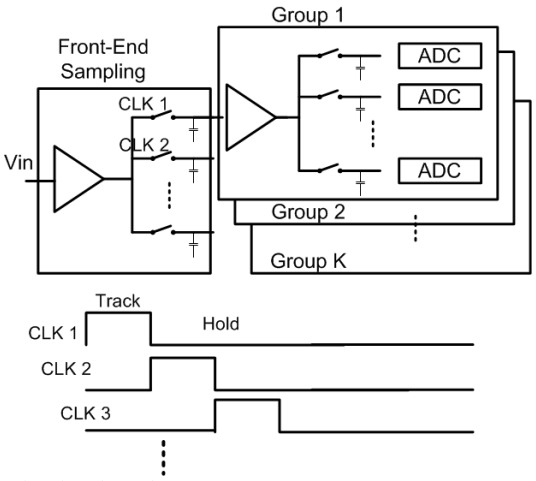

Figure 7 Time interleaved SAR ADC

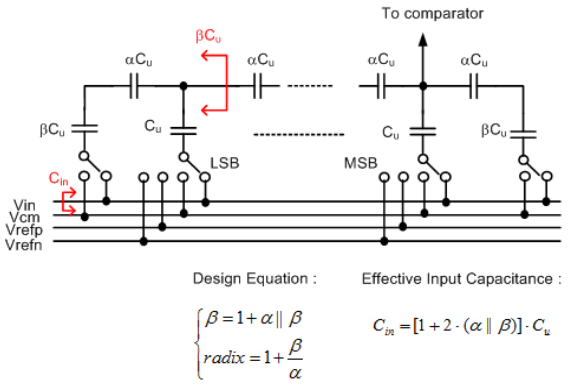

Figure 8 Series capacitor ladder network for S/H

capacitor is activated at a time [34, 35], as shown in Fig. 7. Besides cascading the sampling network, the sampling capacitance of each ADC should be minimized. For a medium resolution ADC, the sampling capacitance is not constrained by the KT/C noise, for instance, an 8-bit ADC requires merely on the order of 10fF total sampling capacitance with 1V input swing. Shown in Fig. 8, a series capacitor ladder network can be applied in both non-binary [16] and binary case [36]. Since the capacitors are connected in series, the total sampling capacitance seen by the input driver is substantially reduced and independent of ADC resolution, which is not the case in the conventional parallel connected capacitor array. Another benefit of using series connected capacitor network is the potential usage of a larger unit capacitor in order to satisfy the matching requirement. Finally, the mismatches between the interleaved ADCs typically require calibrations to compensate for offset, gain, and timing skews [13, 37-39].

VI. CONCLUSION

SAR ADC architecture presents a promising path for high speed and low power operation. Moreover, the nature of its mostly digital implementation will continue to favor the technology scaling in terms of the achievable speed and power consumption. Several outlined techniques, including asynchronous SAR, massive time interleaving, and pipelining, are expected to play a key role in driving even higher sampling rate and lower power consumption in the future. More architecture and circuit level innovations to further enhance SAR conversion speed and reduce the overhead of massive time interleaving are crucial to achieve this goal.

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